

ZZZ1  
PCB

# Compal Confidential

## IFTxx Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M  
(With nVIDIA MXM/B)

2006-11-01

REV: 0.1

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
CARD BUS CB1410	AD20	2	C,D
1394+Cardreader	AD22	0	G,H

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADI ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b	NVIDIA NB8X	

EC SM Bus2 address

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb



Close to CPU pin AD26  
within 500mils.

Width=20 mil

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

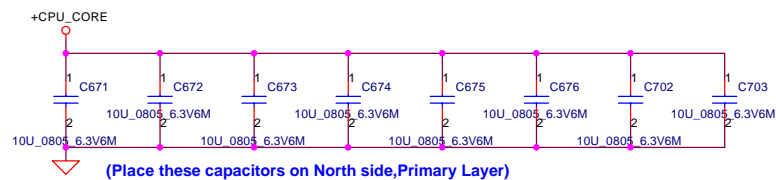
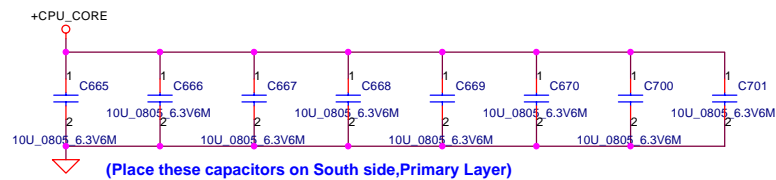
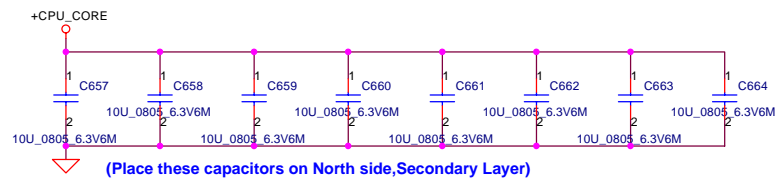
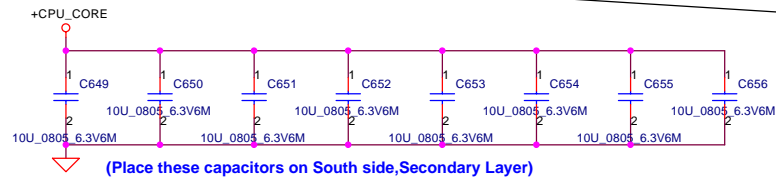
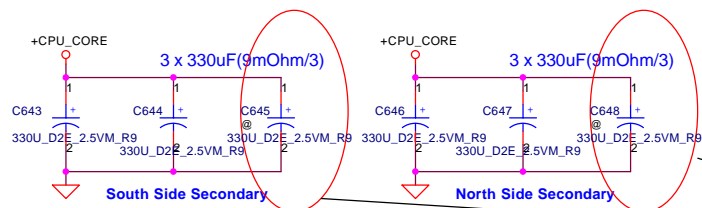
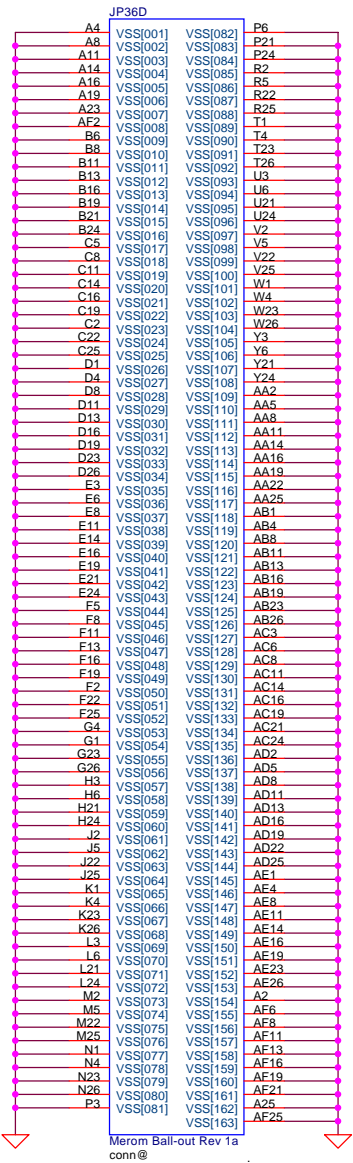
Resistor placed within  
0.5" of CPU pin. Trace  
should be at least 25  
mils away from any other  
toggling signal.  
COMP[0,2] trace width is  
18 mils. COMP[1,3] trace  
width is 4 mils.

Length match within 25 mils.  
The trace width/space/other is  
20/7/25.

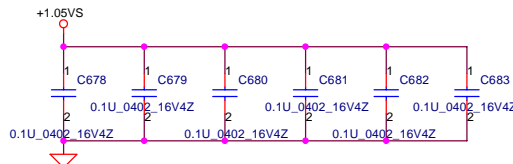
Close to CPU pin  
within 500mils.

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								Merom (2/3)	
								Size B Document Number	
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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



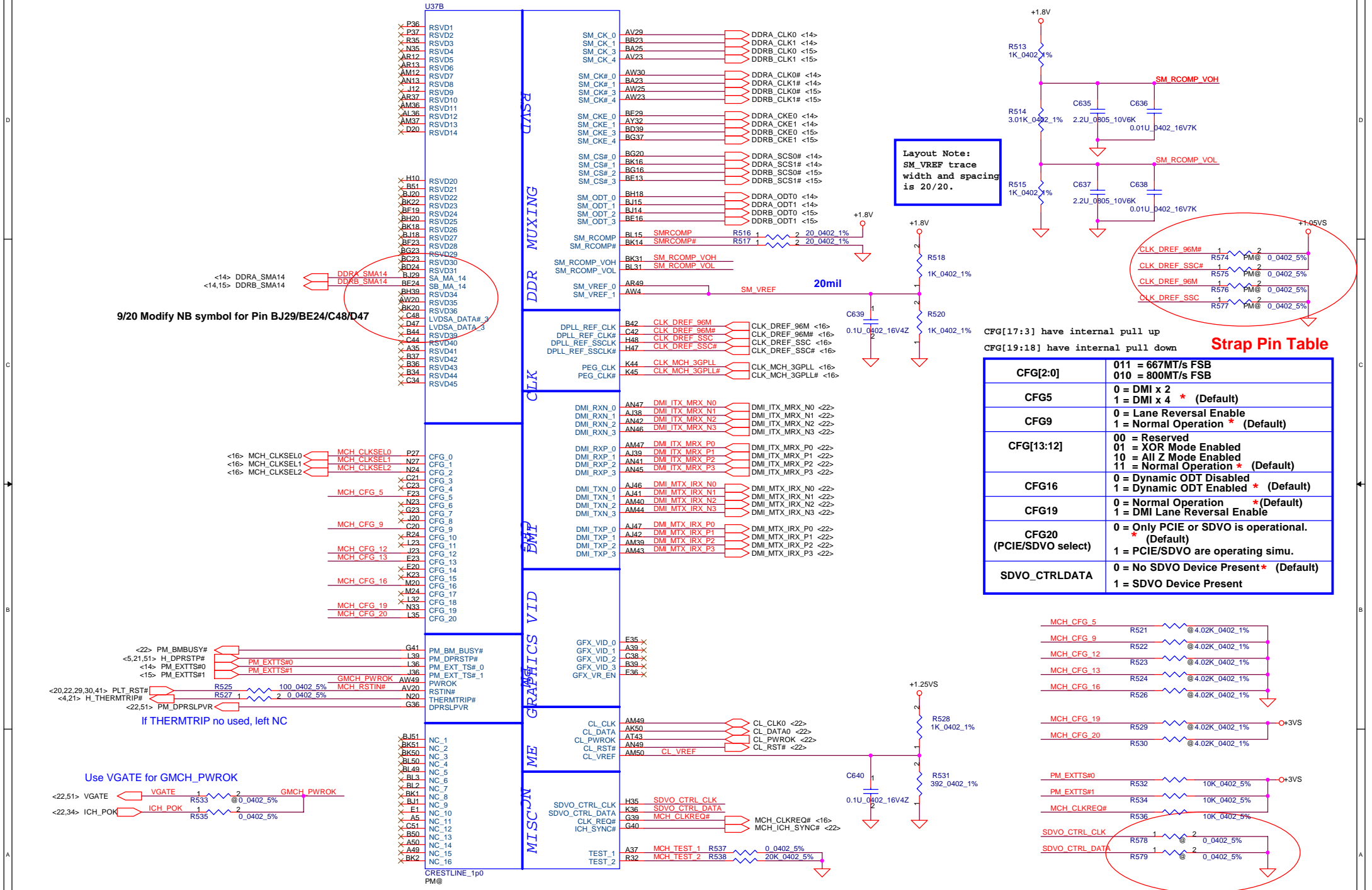
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<14> DDRA\_SDQ[0..63] <--> DDRA\_SDQ[0..63]  
<14> DDRA\_SDM[0..7] <--> DDRA\_SDM[0..7]  
<14> DDRA\_SMA[0..13] <--> DDRA\_SMA[0..13]

<15> DDRB\_SDQ[0..63] <--> DDRB\_SDQ[0..63]  
<15> DDRB\_SDM[0..7] <--> DDRB\_SDM[0..7]  
<15> DDRB\_SMA[0..13] <--> DDRB\_SMA[0..13]

U37D  
DDRA\_SDQ0 AR43 SA\_DQ\_0  
DDRA\_SDQ1 AW44 SA\_DQ\_1  
DDRA\_SDQ2 BA45 SA\_DQ\_2  
DDRA\_SDQ3 AY46 SA\_DQ\_3  
DDRA\_SDQ4 AR41 SA\_DQ\_4  
DDRA\_SDQ5 AR45 SA\_DQ\_5  
DDRA\_SDQ6 AT42 SA\_DQ\_6  
DDRA\_SDQ7 AW47 SA\_DQ\_7  
DDRA\_SDQ8 BB45 SA\_DQ\_8  
DDRA\_SDQ9 BF48 SA\_DQ\_9  
DDRA\_SDQ10 BG47 SA\_DQ\_10  
DDRA\_SDQ11 BA45 SA\_DQ\_11  
DDRA\_SDQ12 BB47 SA\_DQ\_12  
DDRA\_SDQ13 BG50 SA\_DQ\_13  
DDRA\_SDQ14 BH49 SA\_DQ\_14  
DDRA\_SDQ15 BE45 SA\_DQ\_15  
DDRA\_SDQ16 AW44 SA\_DQ\_16  
DDRA\_SDQ17 BA45 SA\_DQ\_17  
DDRA\_SDQ18 BG42 SA\_DQ\_18  
DDRA\_SDQ19 BE40 SA\_DQ\_19  
DDRA\_SDQ20 BF44 SA\_DQ\_20  
DDRA\_SDQ21 BH45 SA\_DQ\_21  
DDRA\_SDQ22 BG40 SA\_DQ\_22  
DDRA\_SDQ23 BE40 SA\_DQ\_23  
DDRA\_SDQ24 AR40 SA\_DQ\_24  
DDRA\_SDQ25 AW40 SA\_DQ\_25  
DDRA\_SDQ26 AT39 SA\_DQ\_26  
DDRA\_SDQ27 AW36 SA\_DQ\_27  
DDRA\_SDQ28 AW41 SA\_DQ\_28  
DDRA\_SDQ29 AY41 SA\_DQ\_29  
DDRA\_SDQ30 AV38 SA\_DQ\_30  
DDRA\_SDQ31 AT38 SA\_DQ\_31  
DDRA\_SDQ32 AV13 SA\_DQ\_32  
DDRA\_SDQ33 AT13 SA\_DQ\_33  
DDRA\_SDQ34 AW11 SA\_DQ\_34  
DDRA\_SDQ35 AY11 SA\_DQ\_35  
DDRA\_SDQ36 AU15 SA\_DQ\_36  
DDRA\_SDQ37 AT11 SA\_DQ\_37  
DDRA\_SDQ38 BA13 SA\_DQ\_38  
DDRA\_SDQ39 BA11 SA\_DQ\_39  
DDRA\_SDQ40 BE10 SA\_DQ\_40  
DDRA\_SDQ41 BD10 SA\_DQ\_41  
DDRA\_SDQ42 BD08 SA\_DQ\_42  
DDRA\_SDQ43 AY9 SA\_DQ\_43  
DDRA\_SDQ44 BG10 SA\_DQ\_44  
DDRA\_SDQ45 AW9 SA\_DQ\_45  
DDRA\_SDQ46 BD7 SA\_DQ\_46  
DDRA\_SDQ47 BB9 SA\_DQ\_47  
DDRA\_SDQ48 BB5 SA\_DQ\_48  
DDRA\_SDQ49 AY7 SA\_DQ\_49  
DDRA\_SDQ50 AT5 SA\_DQ\_50  
DDRA\_SDQ51 AT7 SA\_DQ\_51  
DDRA\_SDQ52 AY6 SA\_DQ\_52  
DDRA\_SDQ53 BB7 SA\_DQ\_53  
DDRA\_SDQ54 AR5 SA\_DQ\_54  
DDRA\_SDQ55 AR8 SA\_DQ\_55  
DDRA\_SDQ56 AR9 SA\_DQ\_56  
DDRA\_SDQ57 AN3 SA\_DQ\_57  
DDRA\_SDQ58 AN8 SA\_DQ\_58  
DDRA\_SDQ59 AN10 SA\_DQ\_59  
DDRA\_SDQ60 AT9 SA\_DQ\_60  
DDRA\_SDQ61 AN9 SA\_DQ\_61  
DDRA\_SDQ62 AM9 SA\_DQ\_62  
DDRA\_SDQ63 AN11 SA\_DQ\_63

CRESTLINE\_1p0  
PM@

DDR SYSTEM MEMORY A

SA\_BS\_0 BB19 <--> DDRA\_SBS0 <14>  
SA\_BS\_1 BK19 <--> DDRA\_SBS1 <14>  
SA\_BS\_2 BF29 <--> DDRA\_SBS2 <14>  
SA\_CAS# BL17 <--> DDRA\_SCAS# <14>  
SA\_DM\_0 AT45 <--> DDRA\_SDM0  
SA\_DM\_1 BD44 <--> DDRA\_SDM1  
SA\_DM\_2 BD42 <--> DDRA\_SDM2  
SA\_DM\_3 AW38 <--> DDRA\_SDM3  
SA\_DM\_4 AW13 <--> DDRA\_SDM4  
SA\_DM\_5 BG8 <--> DDRA\_SDM5  
SA\_DM\_6 AV5 <--> DDRA\_SDM6  
SA\_DM\_7 AN6 <--> DDRA\_SDM7  
SA\_DQS\_0 AT46 <--> DDRA\_SDQS0 <14>  
SA\_DQS\_1 BE48 <--> DDRA\_SDQS1 <14>  
SA\_DQS\_2 BB43 <--> DDRA\_SDQS2 <14>  
SA\_DQS\_3 BC37 <--> DDRA\_SDQS3 <14>  
SA\_DQS\_4 BB16 <--> DDRA\_SDQS4 <14>  
SA\_DQS\_5 BH6 <--> DDRA\_SDQS5 <14>  
SA\_DQS\_6 BB2 <--> DDRA\_SDQS6 <14>  
SA\_DQS\_7 AP3 <--> DDRA\_SDQS7 <14>  
SA\_DQS#\_0 AT47 <--> DDRA\_SDQS#0 <14>  
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SA\_DQS#\_3 BA37 <--> DDRA\_SDQS#3 <14>  
SA\_DQS#\_4 BA16 <--> DDRA\_SDQS#4 <14>  
SA\_DQS#\_5 BH7 <--> DDRA\_SDQS#5 <14>  
SA\_DQS#\_6 BC1 <--> DDRA\_SDQS#6 <14>  
SA\_DQS#\_7 AP2 <--> DDRA\_SDQS#7 <14>  
SA\_MA\_0 BJ19 <--> DDRA\_SMA0  
SA\_MA\_1 BD20 <--> DDRA\_SMA1  
SA\_MA\_2 BK27 <--> DDRA\_SMA2  
SA\_MA\_3 BH28 <--> DDRA\_SMA3  
SA\_MA\_4 BL24 <--> DDRA\_SMA4  
SA\_MA\_5 BK28 <--> DDRA\_SMA5  
SA\_MA\_6 BJ27 <--> DDRA\_SMA6  
SA\_MA\_7 BJ25 <--> DDRA\_SMA7  
SA\_MA\_8 BL28 <--> DDRA\_SMA8  
SA\_MA\_9 BA28 <--> DDRA\_SMA9  
SA\_MA\_10 BC19 <--> DDRA\_SMA10  
SA\_MA\_11 BE28 <--> DDRA\_SMA11  
SA\_MA\_12 BG30 <--> DDRA\_SMA12  
SA\_MA\_13 BJ16 <--> DDRA\_SMA13  
SA\_RAS# BE18 <--> DDRA\_SRAS# <14>  
SA\_RCVEN# AY20 <--> DDRA\_SRCVEN# <14>  
SA\_WE# BA19 <--> DDRA\_SWE# <14>

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DDRB\_SDQ0 AP49 SB\_DQ\_0  
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DDRB\_SDQ2 AW50 SB\_DQ\_2  
DDRB\_SDQ3 AW51 SB\_DQ\_3  
DDRB\_SDQ4 AN51 SB\_DQ\_4  
DDRB\_SDQ5 AN50 SB\_DQ\_5  
DDRB\_SDQ6 AV50 SB\_DQ\_6  
DDRB\_SDQ7 AV49 SB\_DQ\_7  
DDRB\_SDQ8 BA50 SB\_DQ\_8  
DDRB\_SDQ9 BB50 SB\_DQ\_9  
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DDRB\_SDQ11 BE50 SB\_DQ\_11  
DDRB\_SDQ12 BA51 SB\_DQ\_12  
DDRB\_SDQ13 AY49 SB\_DQ\_13  
DDRB\_SDQ14 BF50 SB\_DQ\_14  
DDRB\_SDQ15 BF49 SB\_DQ\_15  
DDRB\_SDQ16 BJ50 SB\_DQ\_16  
DDRB\_SDQ17 BJ44 SB\_DQ\_17  
DDRB\_SDQ18 BJ43 SB\_DQ\_18  
DDRB\_SDQ19 BL43 SB\_DQ\_19  
DDRB\_SDQ20 BK47 SB\_DQ\_20  
DDRB\_SDQ21 BK49 SB\_DQ\_21  
DDRB\_SDQ22 BK43 SB\_DQ\_22  
DDRB\_SDQ23 BK42 SB\_DQ\_23  
DDRB\_SDQ24 BJ41 SB\_DQ\_24  
DDRB\_SDQ25 BL41 SB\_DQ\_25  
DDRB\_SDQ26 BJ37 SB\_DQ\_26  
DDRB\_SDQ27 BJ36 SB\_DQ\_27  
DDRB\_SDQ28 BK41 SB\_DQ\_28  
DDRB\_SDQ29 BJ40 SB\_DQ\_29  
DDRB\_SDQ30 BL36 SB\_DQ\_30  
DDRB\_SDQ31 BK37 SB\_DQ\_31  
DDRB\_SDQ32 BK13 SB\_DQ\_32  
DDRB\_SDQ33 BE11 SB\_DQ\_33  
DDRB\_SDQ34 BK11 SB\_DQ\_34  
DDRB\_SDQ35 BC11 SB\_DQ\_35  
DDRB\_SDQ36 BC13 SB\_DQ\_36  
DDRB\_SDQ37 BE12 SB\_DQ\_37  
DDRB\_SDQ38 BC12 SB\_DQ\_38  
DDRB\_SDQ39 BG12 SB\_DQ\_39  
DDRB\_SDQ40 BJ10 SB\_DQ\_40  
DDRB\_SDQ41 BL9 SB\_DQ\_41  
DDRB\_SDQ42 BK5 SB\_DQ\_42  
DDRB\_SDQ43 BL5 SB\_DQ\_43  
DDRB\_SDQ44 BK9 SB\_DQ\_44  
DDRB\_SDQ45 BK10 SB\_DQ\_45  
DDRB\_SDQ46 BJ8 SB\_DQ\_46  
DDRB\_SDQ47 BL6 SB\_DQ\_47  
DDRB\_SDQ48 BF4 SB\_DQ\_48  
DDRB\_SDQ49 BH5 SB\_DQ\_49  
DDRB\_SDQ50 BG1 SB\_DQ\_50  
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DDRB\_SDQ53 BE4 SB\_DQ\_53  
DDRB\_SDQ54 BD3 SB\_DQ\_54  
DDRB\_SDQ55 BJ2 SB\_DQ\_55  
DDRB\_SDQ56 BA3 SB\_DQ\_56  
DDRB\_SDQ57 BB3 SB\_DQ\_57  
DDRB\_SDQ58 AR1 SB\_DQ\_58  
DDRB\_SDQ59 AT3 SB\_DQ\_59  
DDRB\_SDQ60 AY2 SB\_DQ\_60  
DDRB\_SDQ61 AY3 SB\_DQ\_61  
DDRB\_SDQ62 AU2 SB\_DQ\_62  
DDRB\_SDQ63 AT2 SB\_DQ\_63

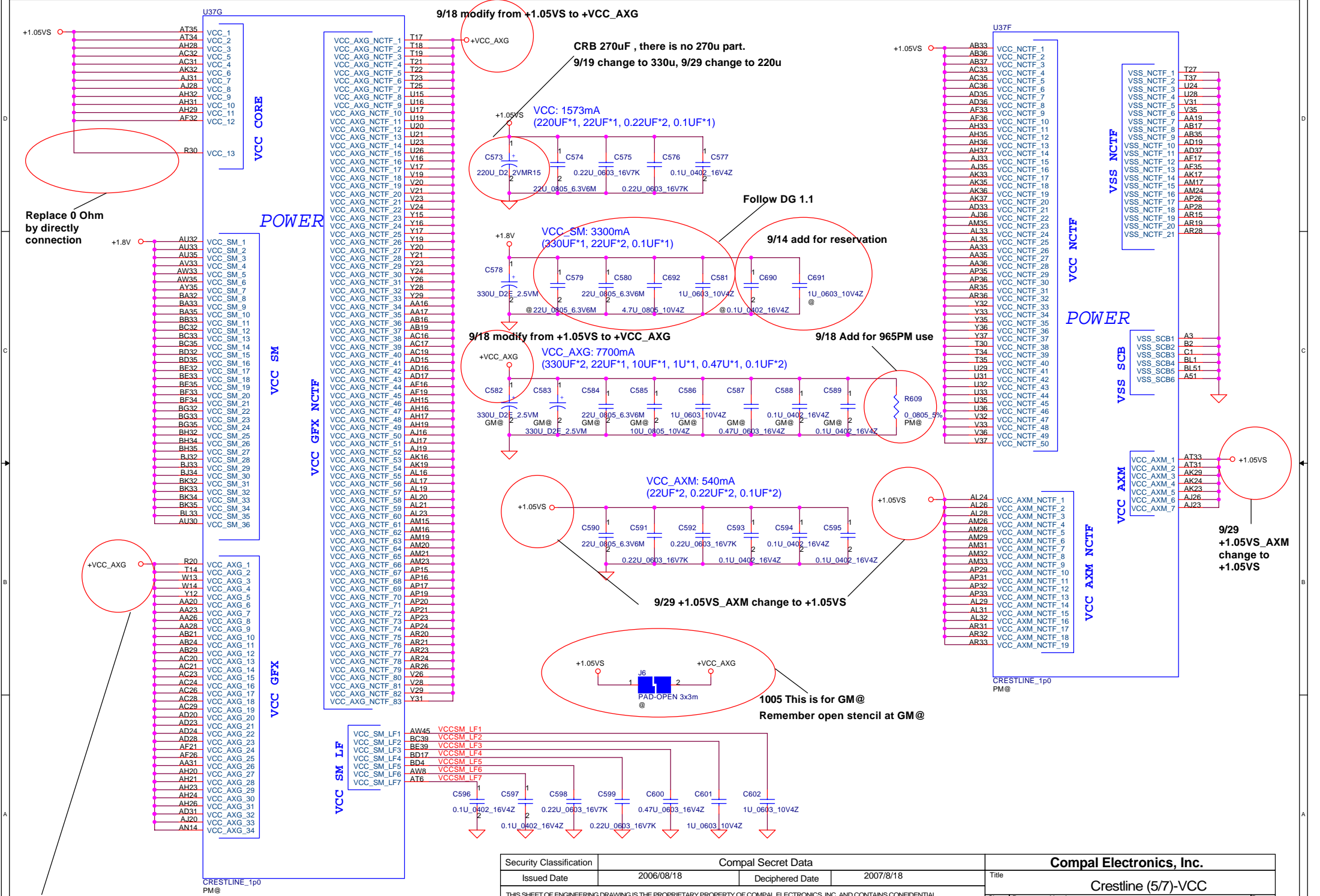
DDR SYSTEM MEMORY B

SB\_BS\_0 AY17 <--> DDRB\_SBS0 <15>  
SB\_BS\_1 BG18 <--> DDRB\_SBS1 <15>  
SB\_BS\_2 BG36 <--> DDRB\_SBS2 <15>  
SB\_CAS# BE17 <--> DDRB\_SCAS# <15>  
SB\_DM\_0 AR50 <--> DDRB\_SDM0  
SB\_DM\_1 BD49 <--> DDRB\_SDM1  
SB\_DM\_2 BK45 <--> DDRB\_SDM2  
SB\_DM\_3 BL39 <--> DDRB\_SDM3  
SB\_DM\_4 BH12 <--> DDRB\_SDM4  
SB\_DM\_5 BJ7 <--> DDRB\_SDM5  
SB\_DM\_6 BF3 <--> DDRB\_SDM6  
SB\_DM\_7 AW2 <--> DDRB\_SDM7  
SB\_DQS\_0 AT50 <--> DDRB\_SDQS0 <15>  
SB\_DQS\_1 BD50 <--> DDRB\_SDQS1 <15>  
SB\_DQS\_2 BK46 <--> DDRB\_SDQS2 <15>  
SB\_DQS\_3 BK39 <--> DDRB\_SDQS3 <15>  
SB\_DQS\_4 BJ12 <--> DDRB\_SDQS4 <15>  
SB\_DQS\_5 BL7 <--> DDRB\_SDQS5 <15>  
SB\_DQS\_6 BE2 <--> DDRB\_SDQS6 <15>  
SB\_DQS\_7 AV2 <--> DDRB\_SDQS7 <15>  
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SB\_DQS#\_1 BC50 <--> DDRB\_SDQS#1 <15>  
SB\_DQS#\_2 BL45 <--> DDRB\_SDQS#2 <15>  
SB\_DQS#\_3 BK38 <--> DDRB\_SDQS#3 <15>  
SB\_DQS#\_4 BK12 <--> DDRB\_SDQS#4 <15>  
SB\_DQS#\_5 BK7 <--> DDRB\_SDQS#5 <15>  
SB\_DQS#\_6 BF2 <--> DDRB\_SDQS#6 <15>  
SB\_DQS#\_7 AV3 <--> DDRB\_SDQS#7 <15>  
SB\_MA\_0 BC18 <--> DDRB\_SMA0  
SB\_MA\_1 BG28 <--> DDRB\_SMA1  
SB\_MA\_2 BG25 <--> DDRB\_SMA2  
SB\_MA\_3 AW17 <--> DDRB\_SMA3  
SB\_MA\_4 BE25 <--> DDRB\_SMA4  
SB\_MA\_5 BE25 <--> DDRB\_SMA5  
SB\_MA\_6 BA29 <--> DDRB\_SMA6  
SB\_MA\_7 BC28 <--> DDRB\_SMA7  
SB\_MA\_8 AY28 <--> DDRB\_SMA8  
SB\_MA\_9 BD37 <--> DDRB\_SMA9  
SB\_MA\_10 BG17 <--> DDRB\_SMA10  
SB\_MA\_11 BE37 <--> DDRB\_SMA11  
SB\_MA\_12 BA39 <--> DDRB\_SMA12  
SB\_MA\_13 BG13 <--> DDRB\_SMA13  
SB\_RAS# AV16 <--> DDRB\_SRAS# <15>  
SB\_RCVEN# AY18 <--> DDRB\_SRCVEN# <15>  
SB\_WE# BC17 <--> DDRB\_SWE# <15>

CRESTLINE\_1p0  
PM@

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Size B	Document Number IFTXX M/B LA-3541P Schematic			Rev 0	
Date:	Wednesday, November 01, 2006	Sheet 9	of 52		

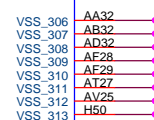




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Size	Document Number	IFTXX M/B LA-3541P Schematic		Rev	
B	0	Date: Wednesday, November 01, 2006		Sheet 11 of 52	

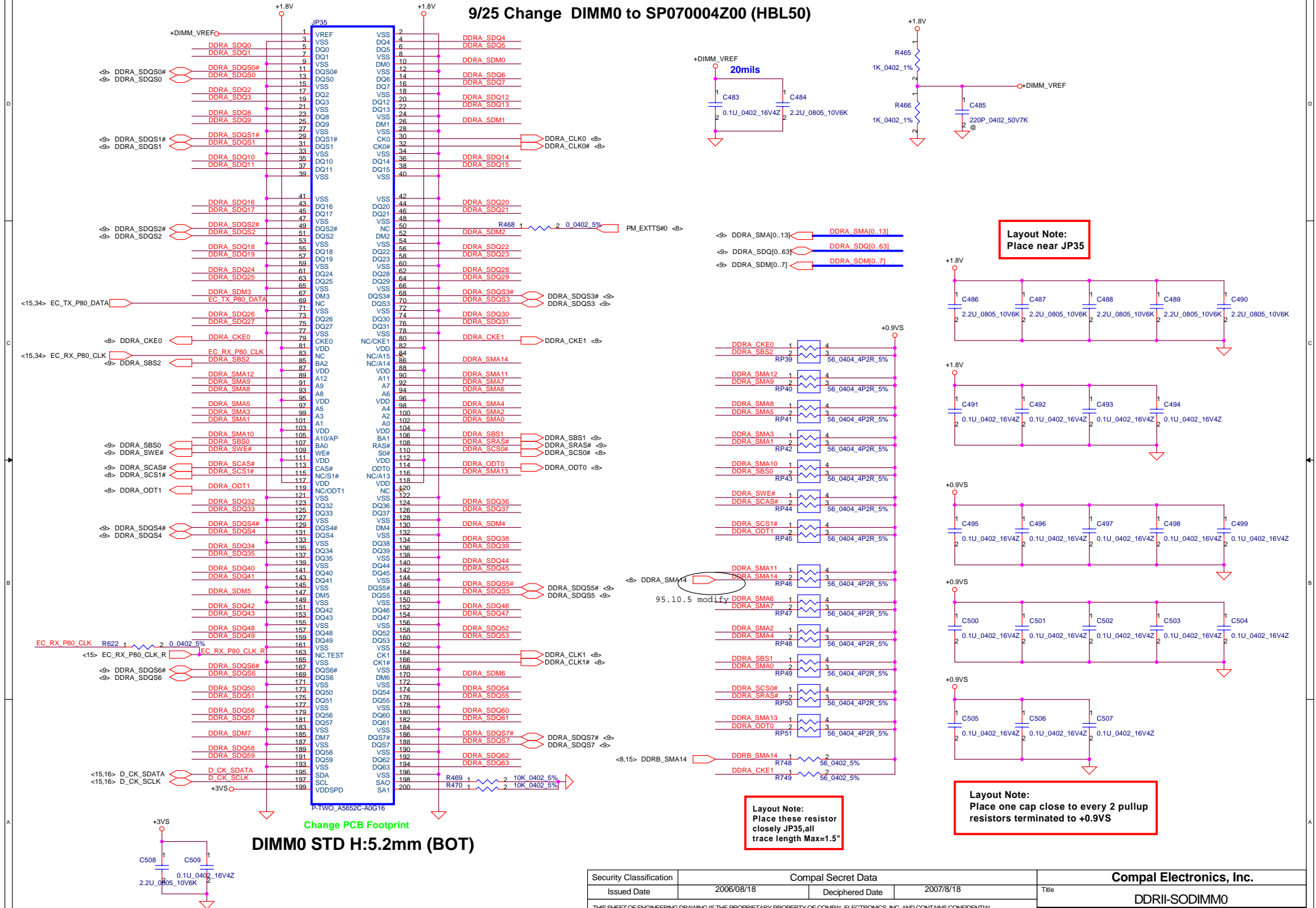






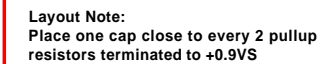
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Crestline (7/7)-GND	
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Date: Wednesday, November 01, 2006				Sheet	13	of 52

+1.8V



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		Size B	Document Number			Rev 0
		IFTXX M/B LA-3541P Schematic				
		Date:	Wednesday, November 01, 2006	Sheet	14	of 52

**DIMM1 STD H:9.2mm (BOT)**







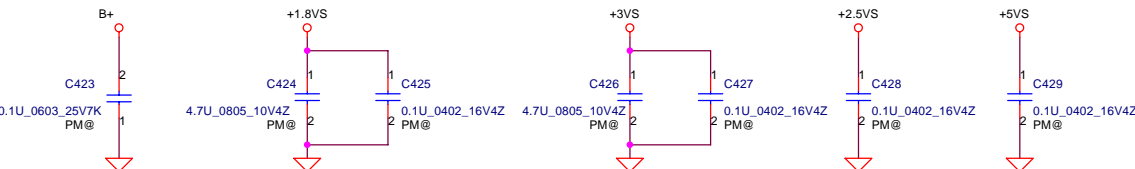
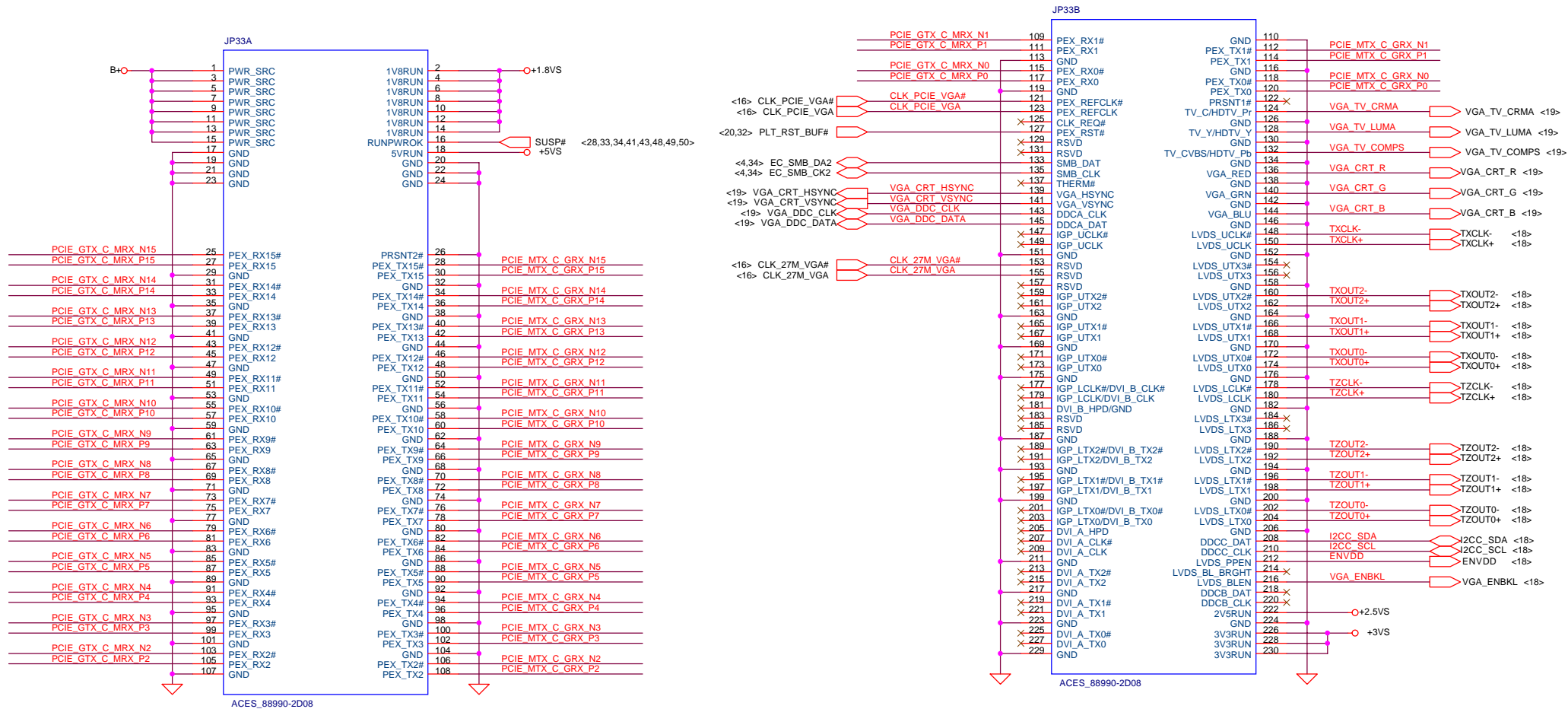
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		Size	Document Number						Rev	
		IFTXX M/B LA-3541P Schematic								0
		Date:	Wednesday, November 01, 2006			Sheet	15		of	52





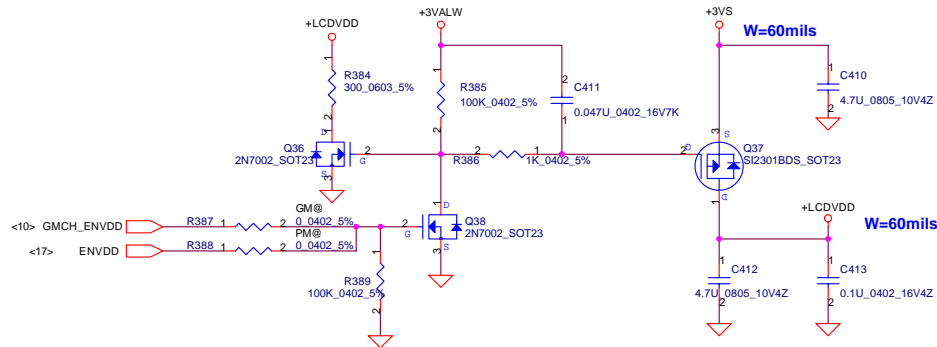
# 9/13 modify this footprint from ACES\_88990-2D08\_230P to ACES\_88990-2D28\_230P

<10> PCIE\_MTX\_C\_GRX\_N[0..15]  PCIE\_MTX\_C\_GRX\_N[0..15]  
 <10> PCIE\_MTX\_C\_GRX\_P[0..15]  PCIE\_MTX\_C\_GRX\_P[0..15]  
 <10> PCIE\_GTX\_C\_MRX\_N[0..15]  PCIE\_GTX\_C\_MRX\_N[0..15]  
 <10> PCIE\_GTX\_C\_MRX\_P[0..15]  PCIE\_GTX\_C\_MRX\_P[0..15]

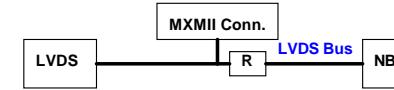


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
Custpm	IFTXX M/B LA-3541P Schematic	0		Wednesday, November 01, 2006	
Sheet		17		of 52	

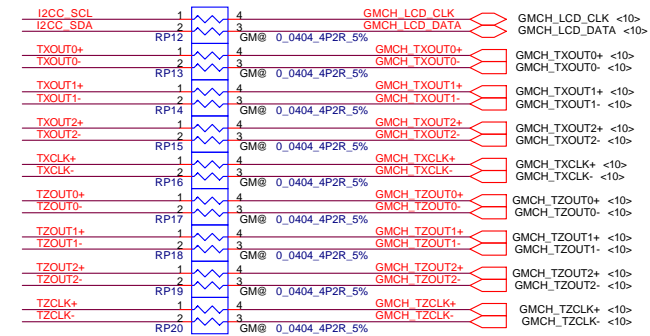
# LCD POWER CIRCUIT



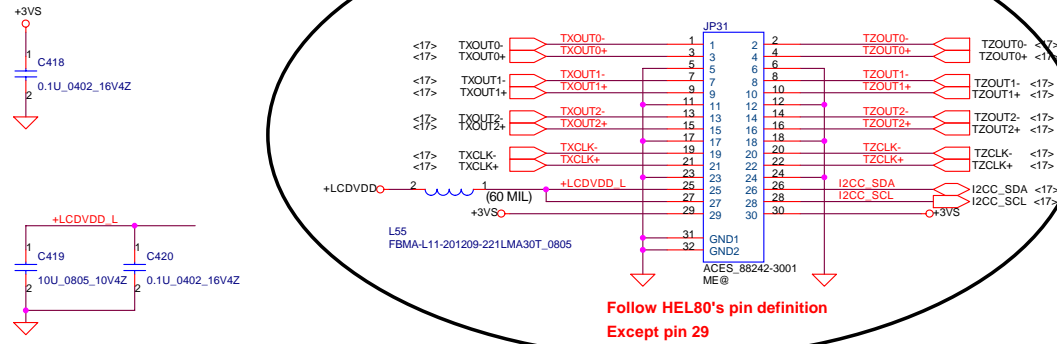
## Routing Diagram



Use Daisy chain to route

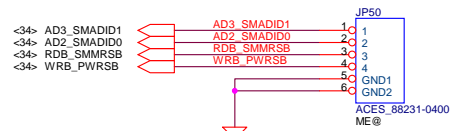


## LCD/PANEL BD. Conn.

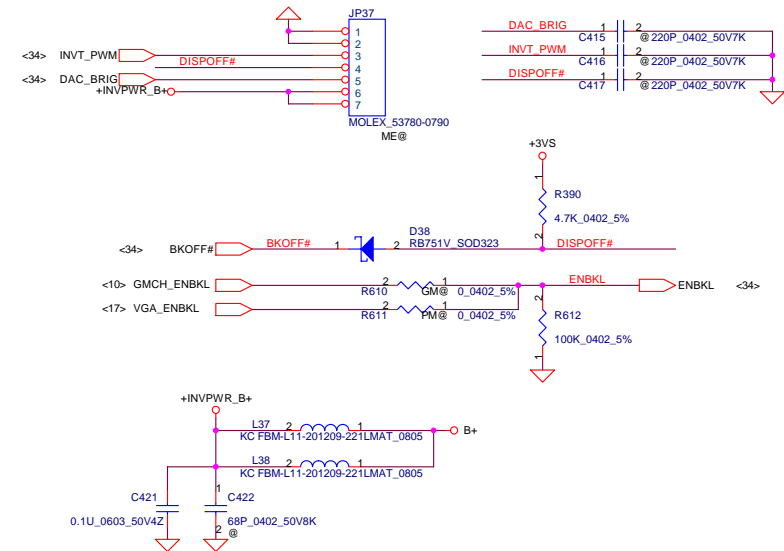


Follow HEL80's pin definition  
Except pin 29

## JEPICO Conn.

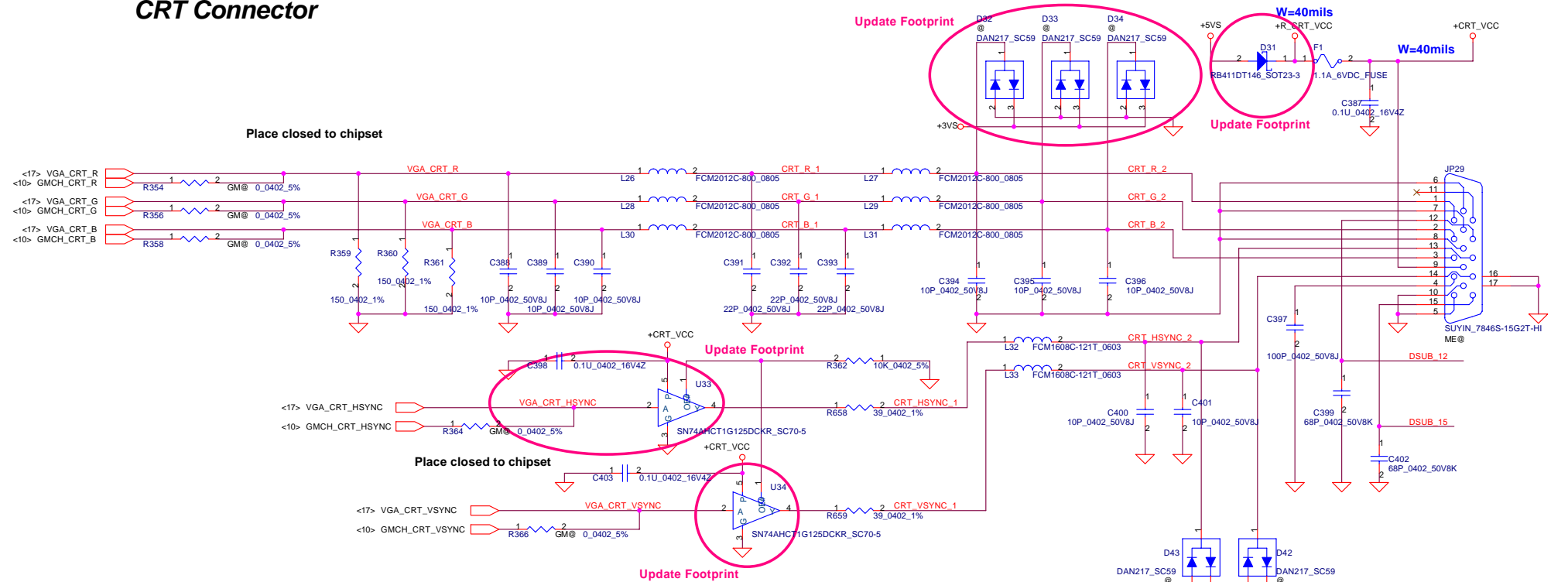
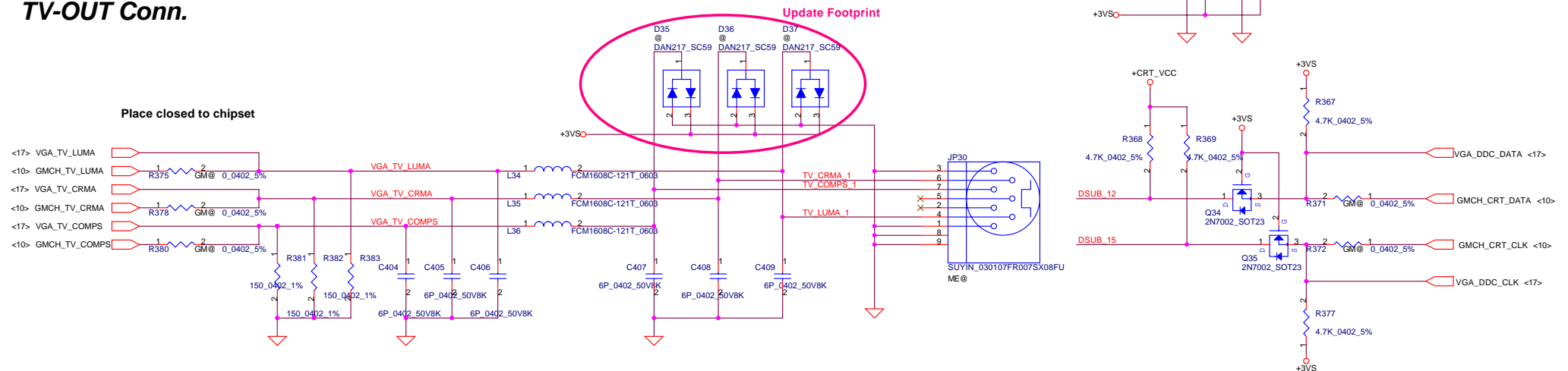


## INVERTER Conn.

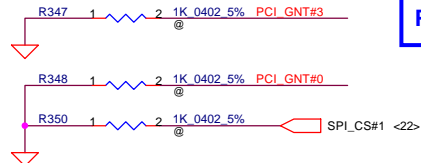
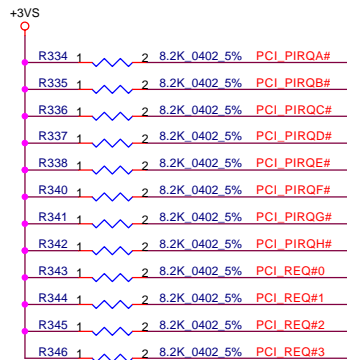
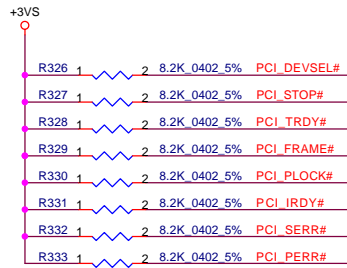


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				IFTXX/MB LA-3541P Schematic	
				Date: Wednesday, November 01, 2006	Sheet 18 of 52

## CRT Connector

**TV-OUT Conn.**

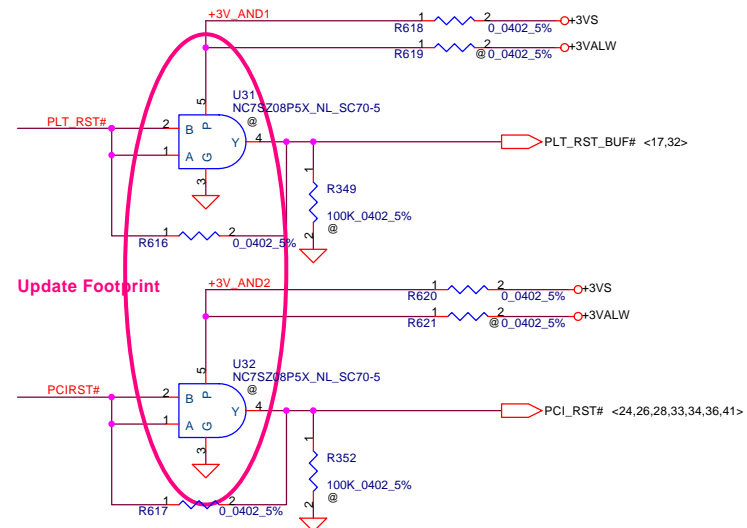
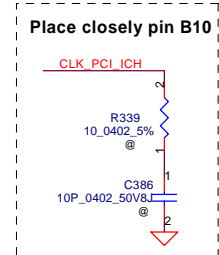
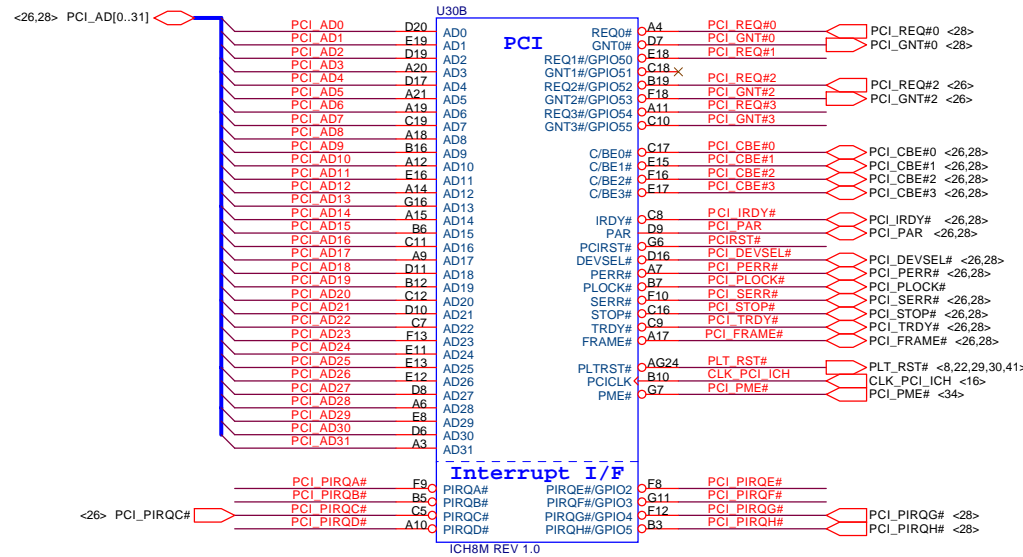
Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	CRT & TV-OUT Connector		
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				IFTXX M/B LA-3541P Schematic			
				Date:	Wednesday, November 01, 2006	Sheet	19 of 52

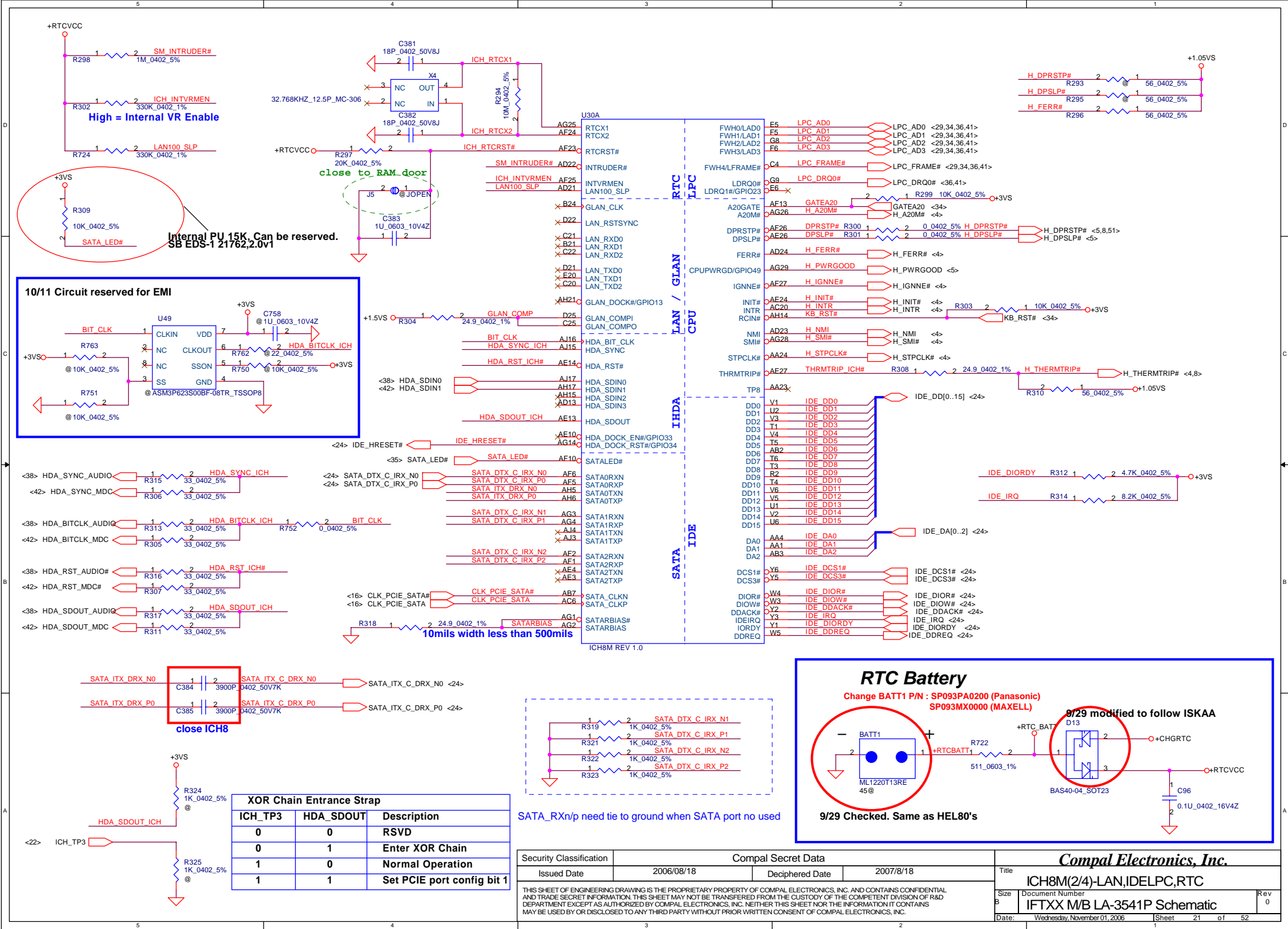


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

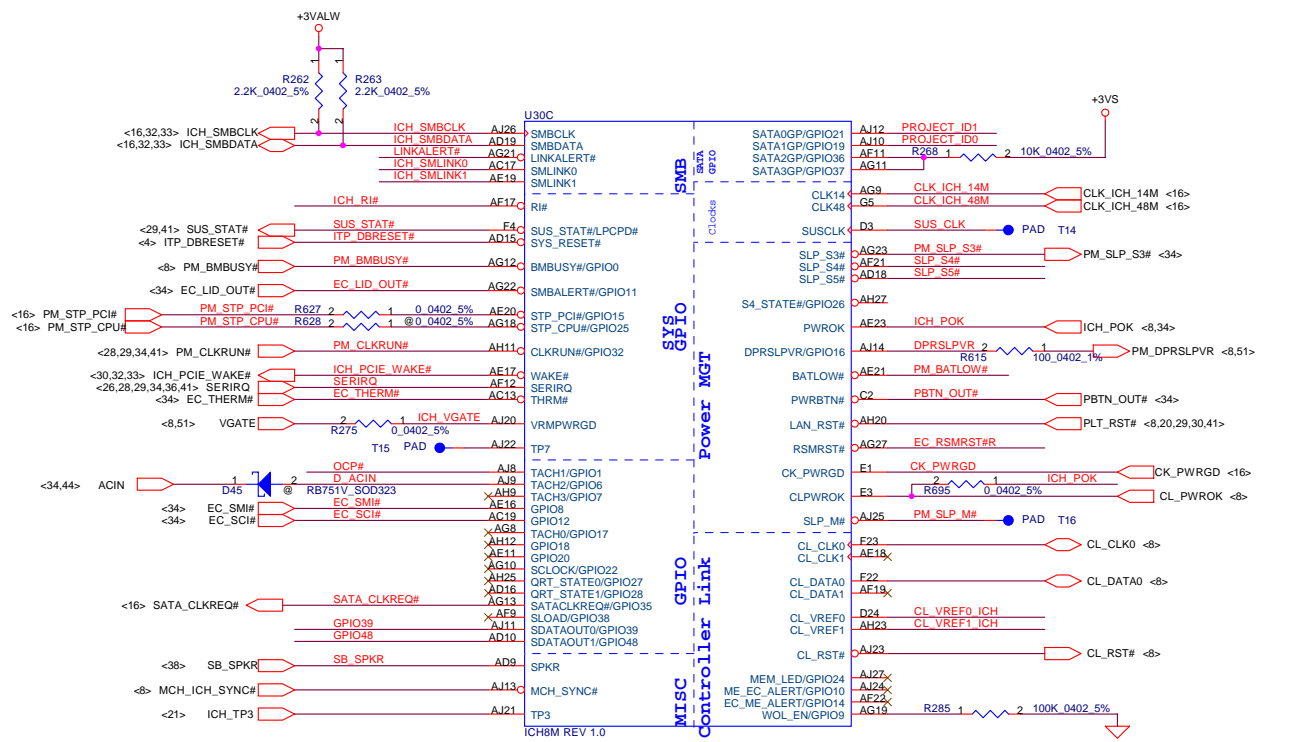
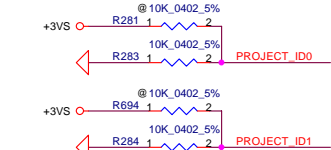
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

10/17 : Change P/N from SA000010G00 to SA00001JU10  
 10/17 : FootPrint : SA000010G00  
 BOM : SA00001JU10









LAN

NEW Card

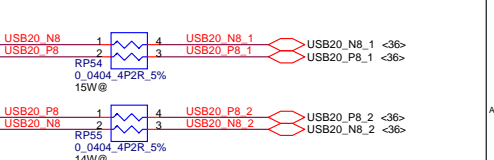
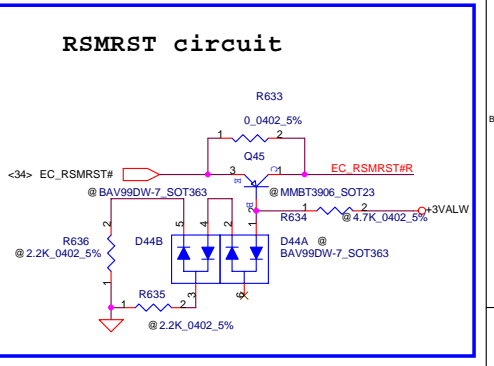
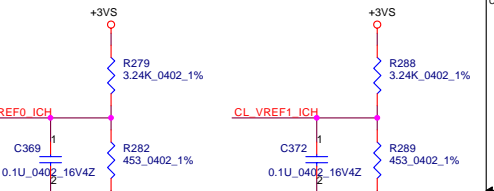
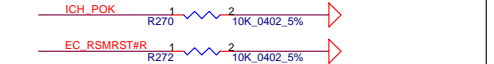
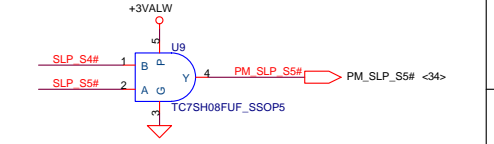
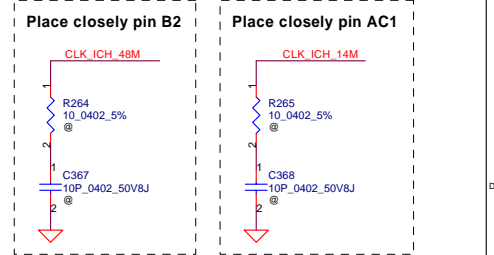
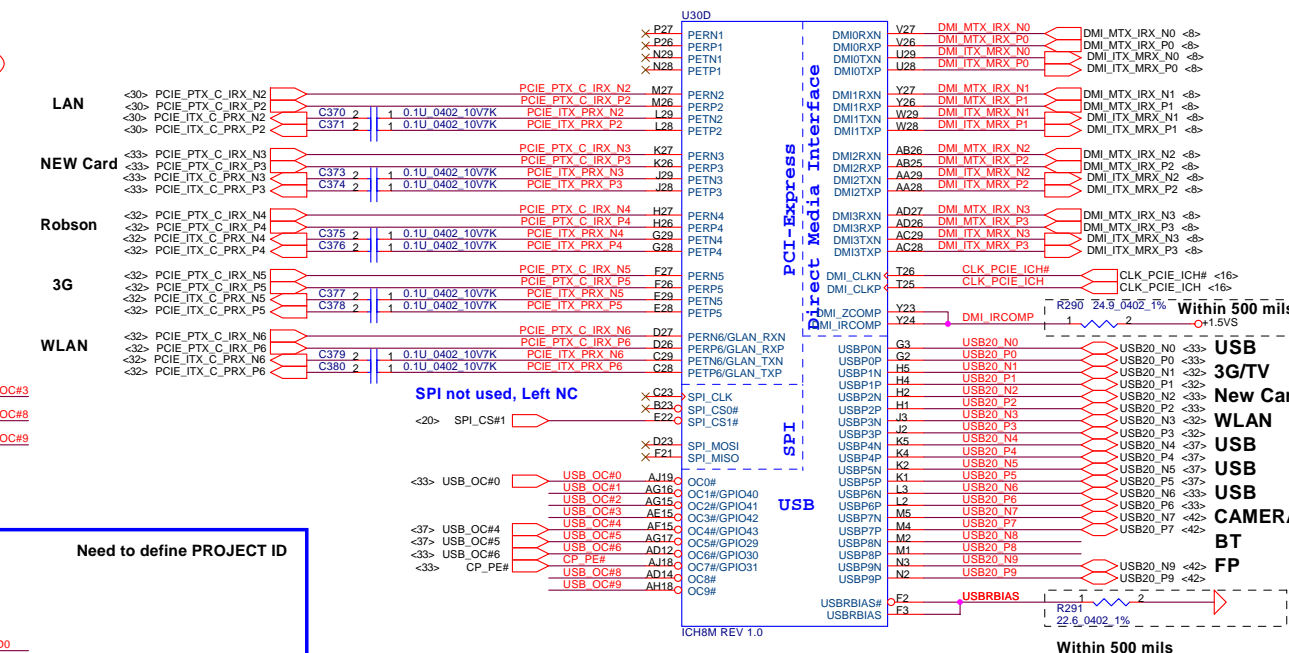
**Robson**

### 3G

WLAN

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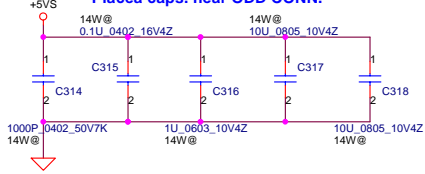
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH8M(34)-USB,GPIO,PCIE	
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				IFTXX MB LA-3541P Schematic		
				Date:	Wednesday, November 01, 2006	Sheet



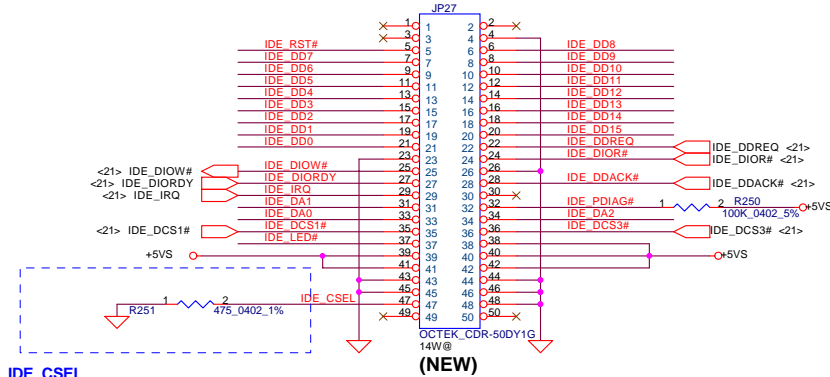


## 14W ODD Conn.

Place caps. near ODD CONN.



<21> IDE\_DD[0..15] IDE\_DD[0..15]  
<21> IDE\_DA[0..2] IDE\_DA[0..2]

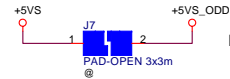


IDE\_CSEL  
Grounding for Master (When use SATA HDD)  
Open or High for Slaver (Normal)

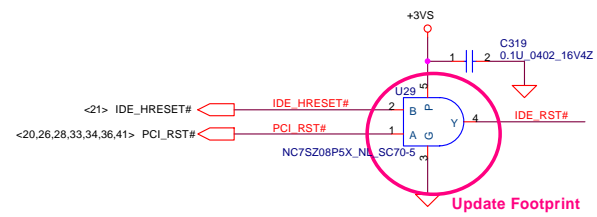
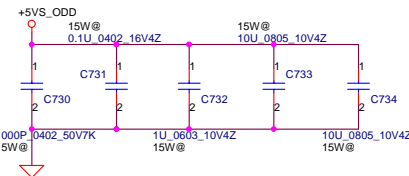
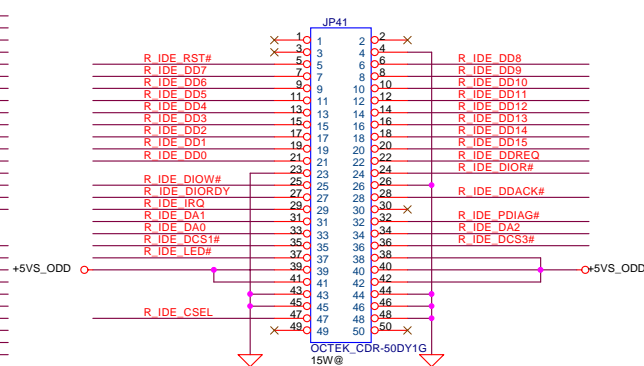
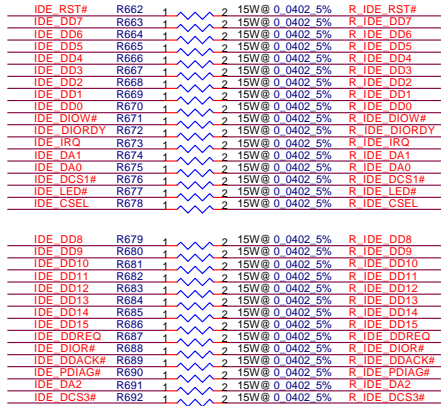
(NEW)

+5VS R252 100K 0402 5%

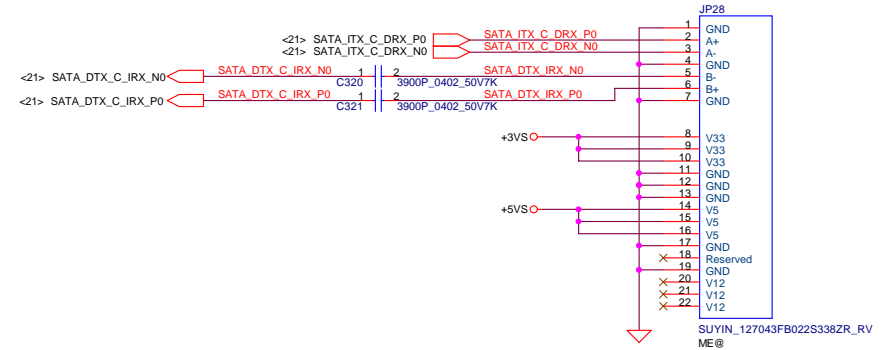
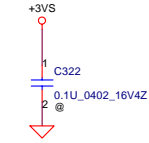
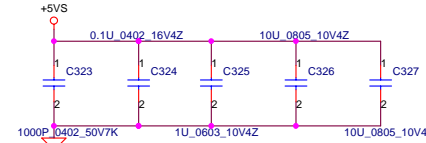
## 15W ODD Conn.



Remember Short at 15W@



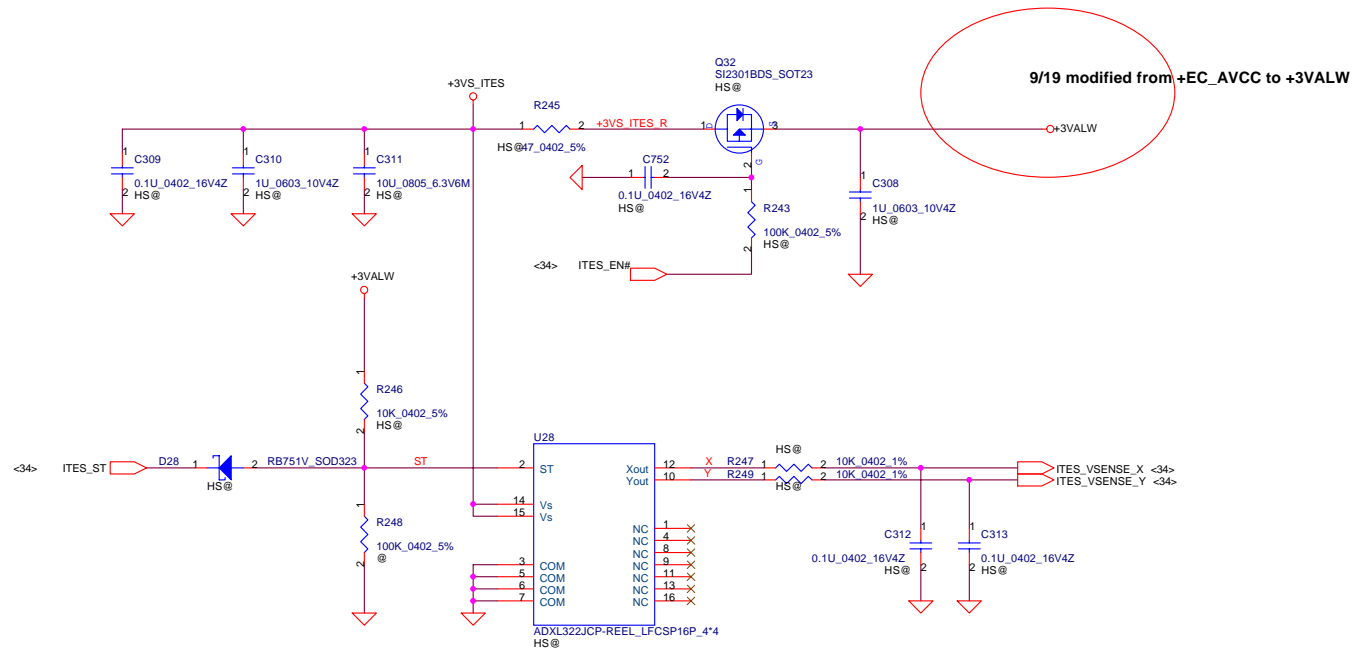
## SATA HDD Conn.



(NEW)  
Change Library

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Size B	Document Number	IFTXX M/B LA-3541P Schematic		Rev 0	
Date:	Wednesday, November 01, 2006	Sheet	24	of 52	

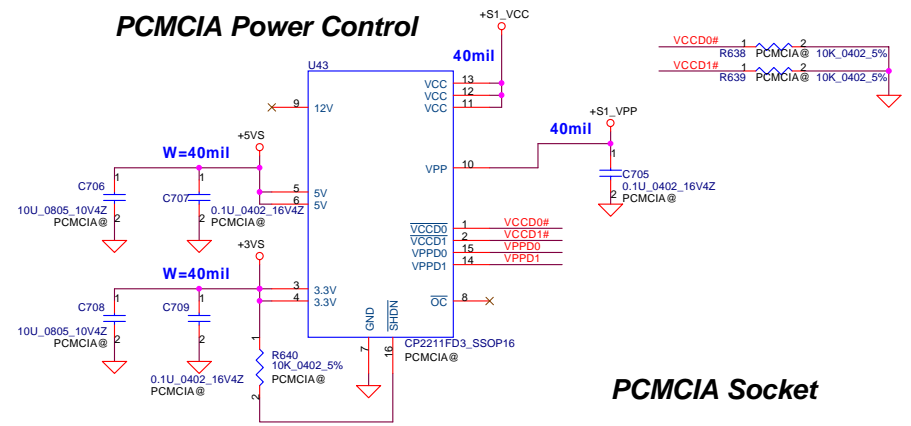
**Note : BOM structure HS@ is for Heng shan IFT10/11 this model**



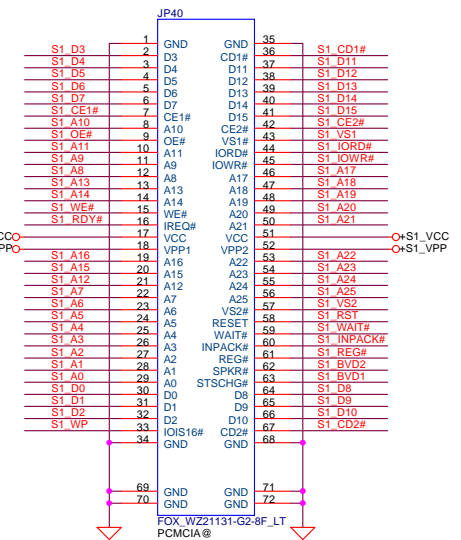
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Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	
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				LA-3541P	
				Date:	Wednesday, November 01, 2006
				Sheet	25 of 52
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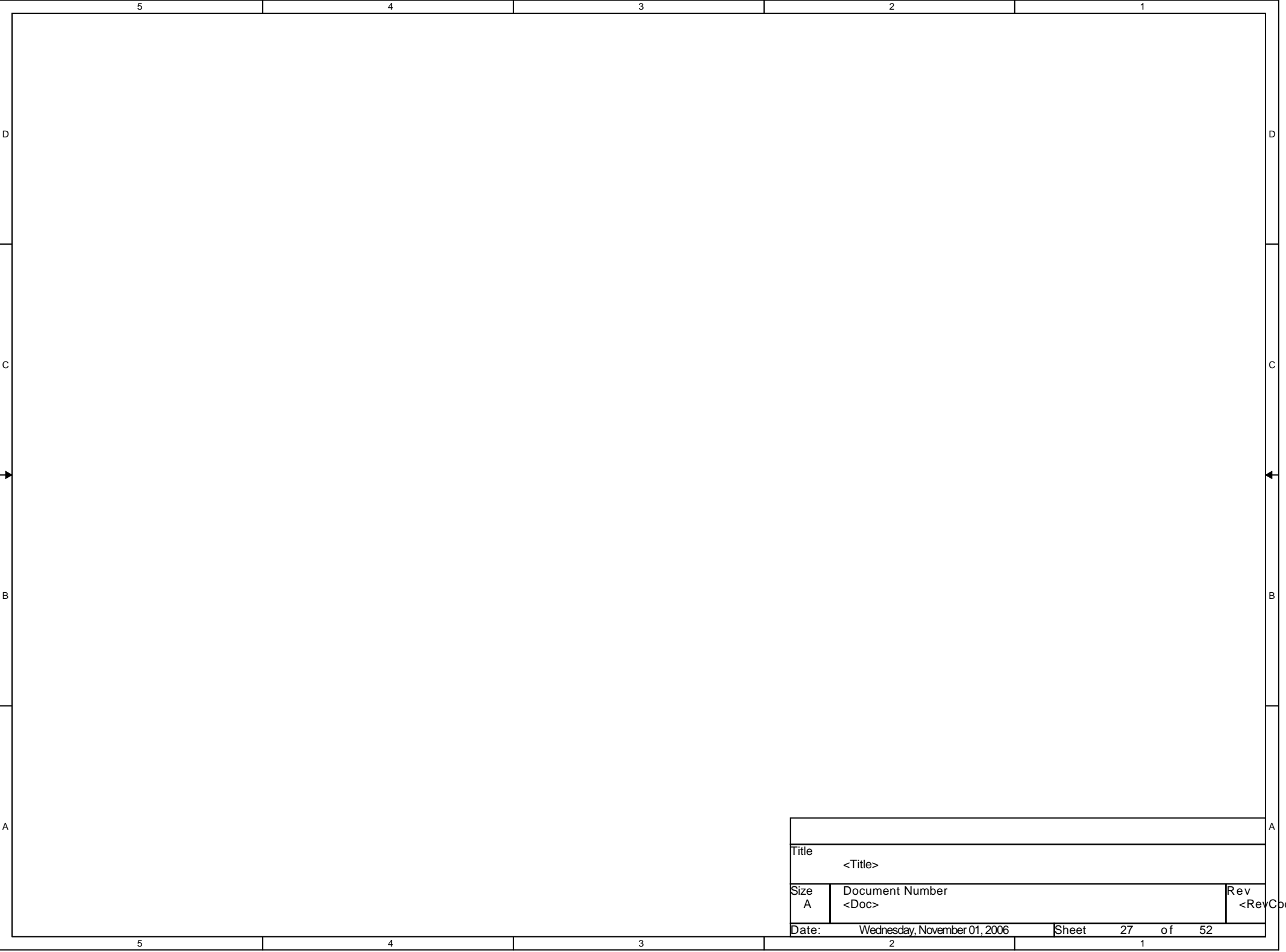
## PCMCIA Power Control

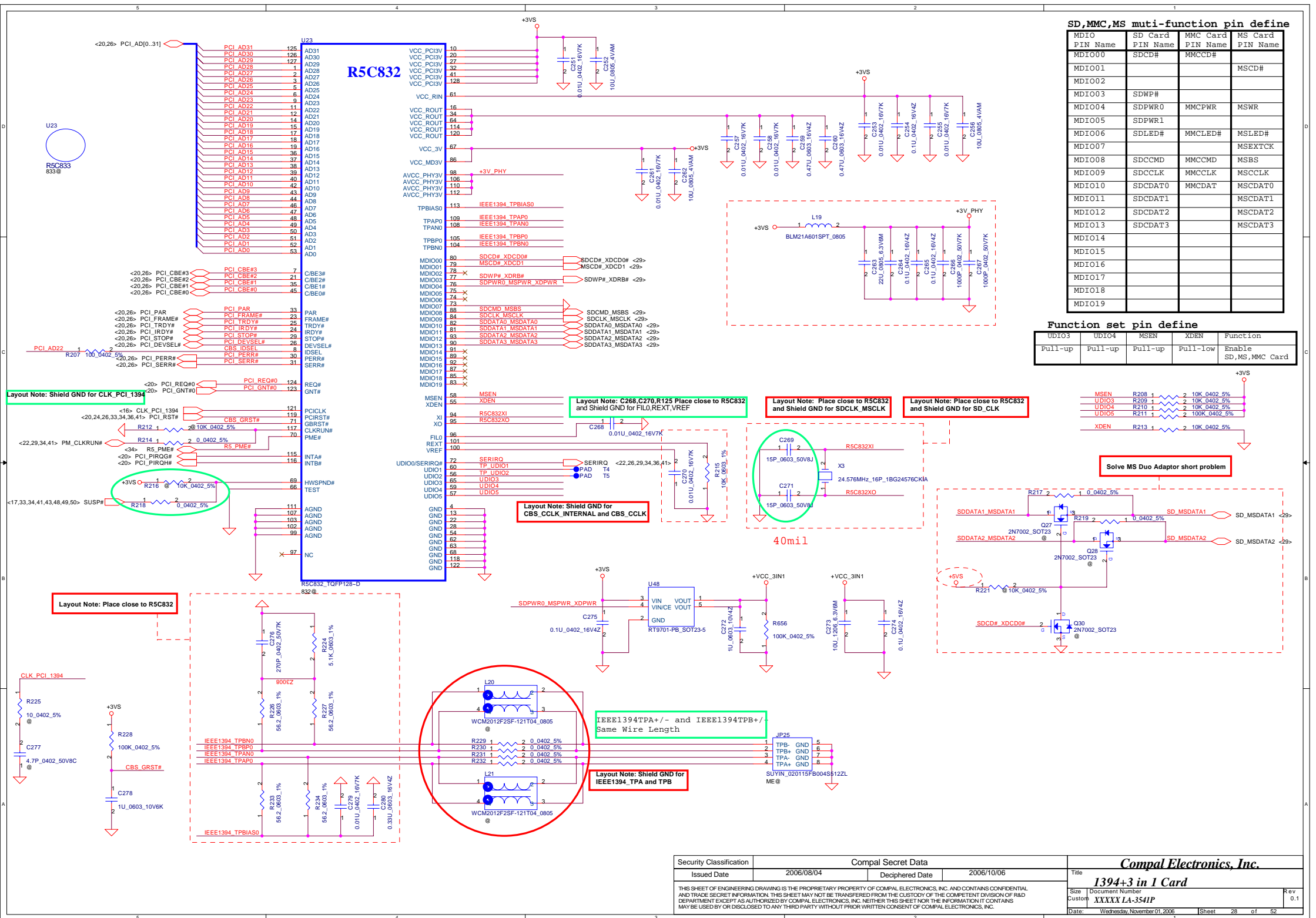


## PCMCIA Socket



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	PCMCIA ENE CB1410	Size	Document Number
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Pin connection diagram for the PROCO\_MDR019-C0-1202 ME@ module. The diagram shows connections for JP24, JP25, and JP26. JP24 (pins 6-8) connects VDD\_SD, DAT0\_SD, DAT1\_SD, DAT2\_SD, CDAT03\_SD, CLK\_SD, WP\_SD, CMD\_SD, CD\_SD, VSS\_SD, and VSS\_SD. JP25 (pins 19-23) connects VCC\_MS, SCLK\_MS, SCLK\_MS, INS\_MS, SDIO\_MS, BS\_MS, RESERVED\_MS, RESERVED\_MS, VSS\_MS, VSS\_MS, GND, and GND. JP26 (pins 1-4) connects SDDATA0\_MSDATA0, SD\_MSDATA1, SD\_MSDATA2, SDDATA3\_MSDATA3, SDCLK\_MSCLK, SDWP#\_XDRB#, SDCMD\_MSBS, and SDCD#\_XDCDD#. The diagram also shows internal connections for SDDATA0\_MSDATA0, SD\_MSDATA1, SD\_MSDATA2, SDDATA3\_MSDATA3, SDCLK\_MSCLK, SDWP#\_XDRB#, SDCMD\_MSBS, SDCD#\_XDCDD#, SDDATA1\_MSDATA1, MSCD#\_XDCD1, SDDATA0\_MSDATA0, SDCMD\_MSBS, SDDATA3\_MSDATA3, and SDDATA2\_MSDATA2. A 10k resistor is connected between pins 1 and 2 of JP25.

### For A30

Diagram showing the connection for Pin 19 (PM\_CLKR#) of the ACES 88019-2000 ME@ chip. The chip is labeled JP47. The connections are as follows:

- Pin 1: SUS\_STAT#
- Pin 2: SERIRQ
- Pin 3: TPM\_TEST1
- Pin 4: (unconnected)
- Pin 5: (unconnected)
- Pin 6: (unconnected)
- Pin 7: (unconnected)
- Pin 8: (unconnected)
- Pin 9: (unconnected)
- Pin 10: (unconnected)
- Pin 11: (unconnected)
- Pin 12: (unconnected)
- Pin 13: (unconnected)
- Pin 14: (unconnected)
- Pin 15: PLT\_RST#
- Pin 16: PM\_CLKR#
- Pin 17: (unconnected)
- Pin 18: (unconnected)
- Pin 19: PM\_CLKR#
- Pin 20: (unconnected)

The chip is connected to the following signals:

- LPC\_AD0
- LPC\_AD1
- LPC\_FRAME#
- CLK\_PCI\_TPM
- LPC\_AD2
- LPC\_AD3

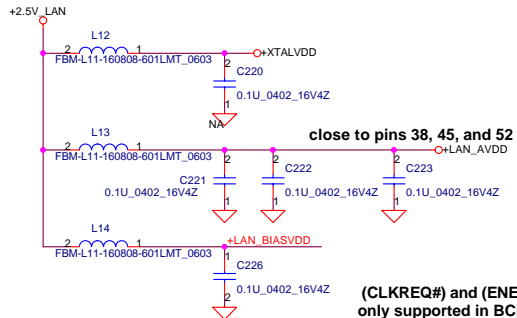
A red circle highlights a 10uF 0805 capacitor (C739) connected between pin 19 and ground. The capacitor is labeled C739 and 10U\_0805 10V4V.

**Place this cap close to pin 6 and pin 9**

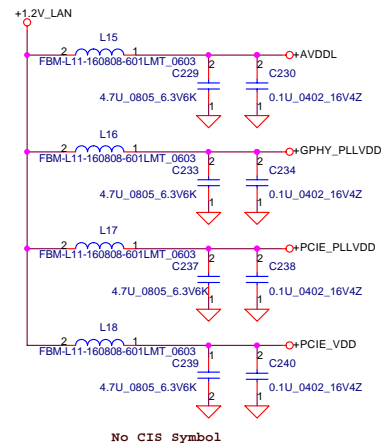
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title <b>INDICATE LED</b>		
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					XXXXX LA-354IP	0.1
				Date:	Wednesday, November 01, 2006	Sheet



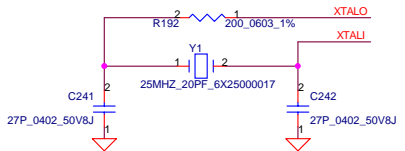
Layout Notice : Filter place as close chip as possible.



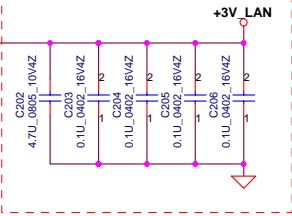
(CLKREQ#) and (ENERGY\_DET) are only supported in BCM5787M



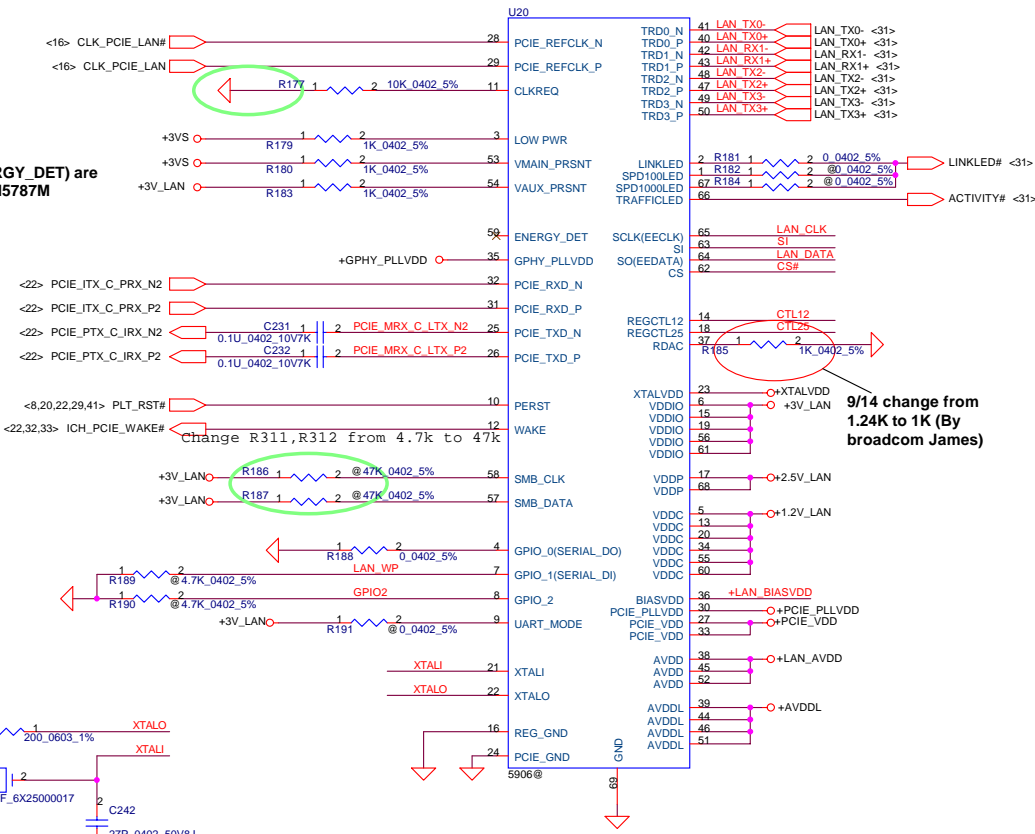
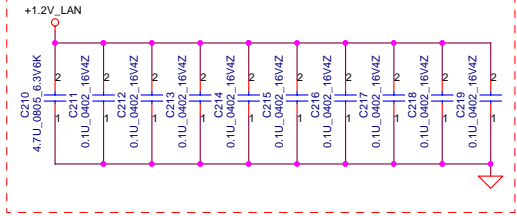
No CIS Symbol



Layout Notice : Place as close chip as possible.

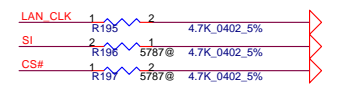
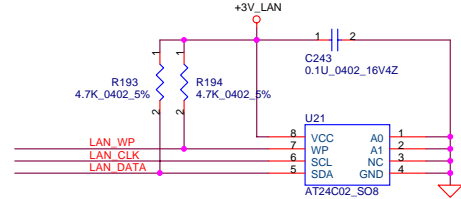
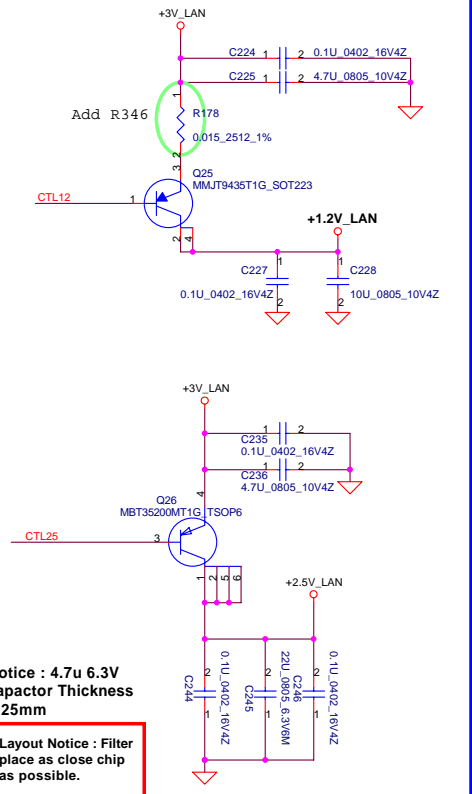


Layout Notice : 1.2V filter. Place as close chip as possible.

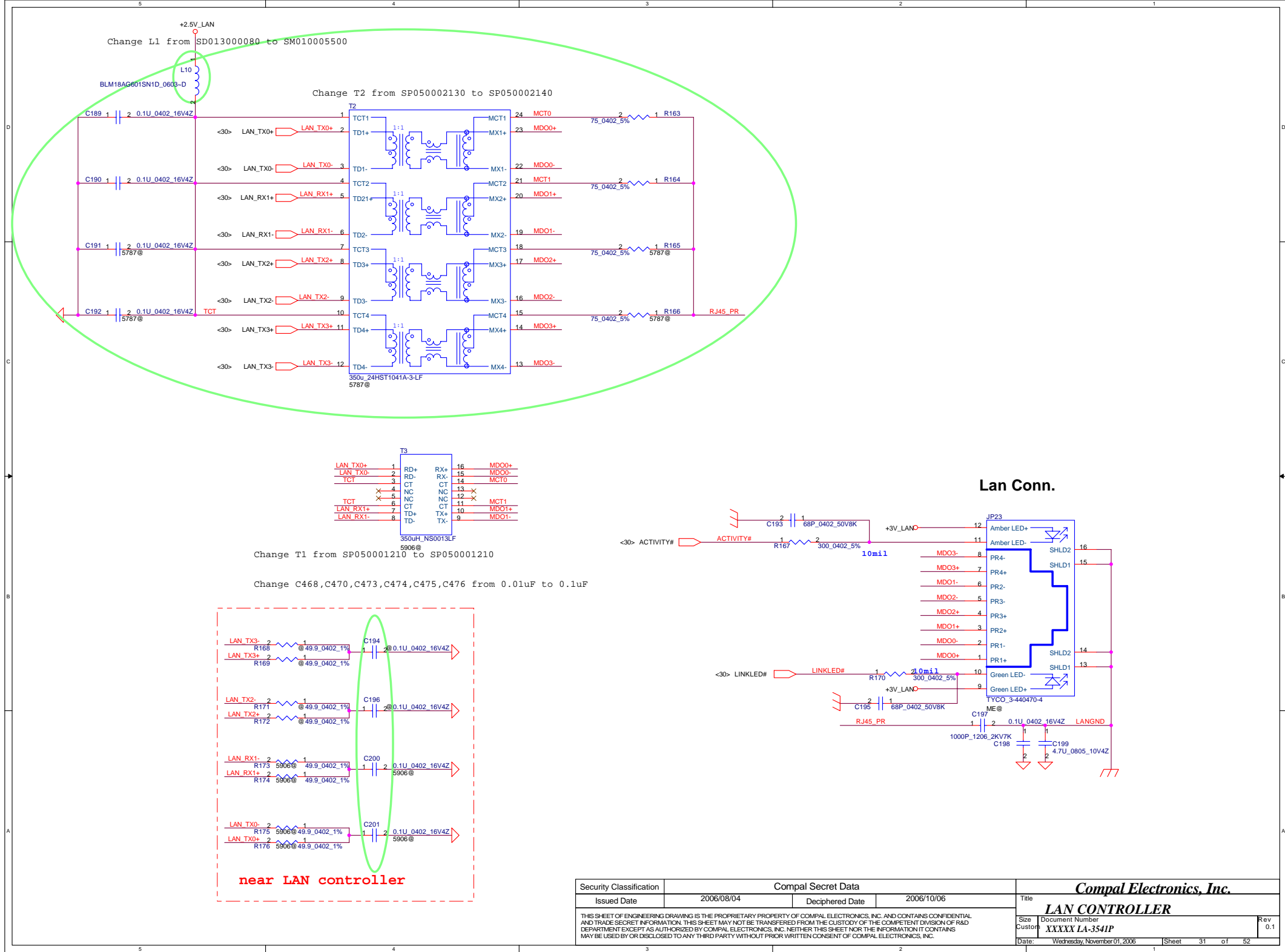


9/14 change from 1.24K to 1K (By broadcom James)

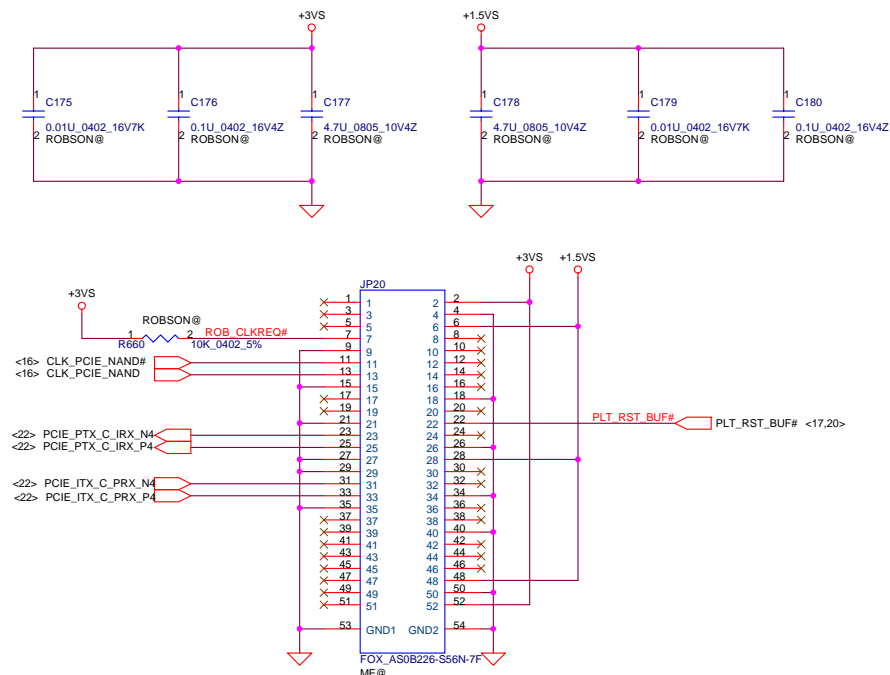
Notice : 4.7u 6.3V capacitor Thickness 1.25mm  
Layout Notice : Filter place as close chip as possible.



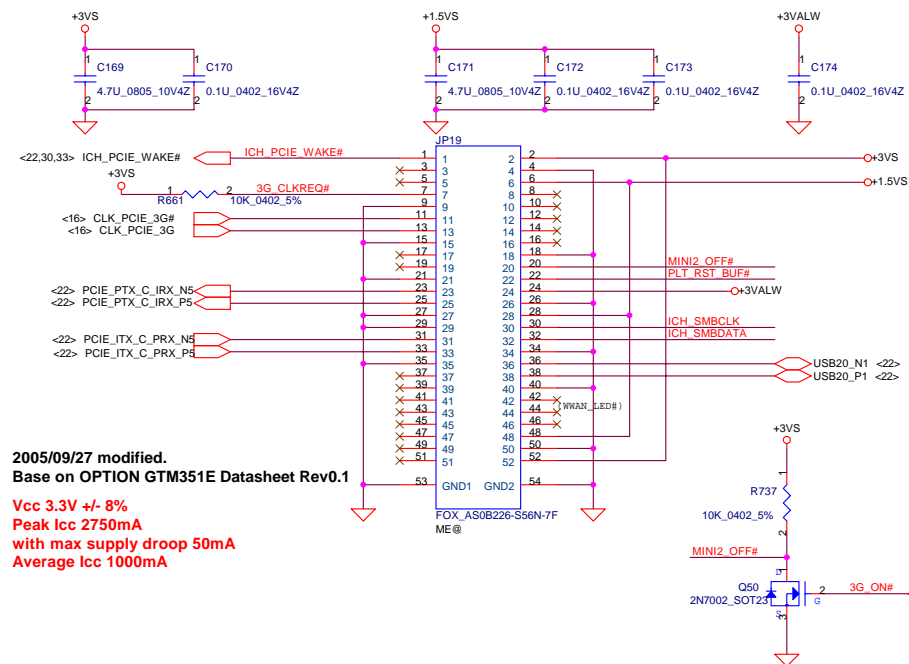
Security Classification		Compal Secret Data							
Issued Date		2006/08/04		Deciphered Date		2006/10/06		Title	
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						Size	Document Number		Rev
						Customer	XXXXX LA-3541P		0.1
						Date:	Wednesday, November 01, 2006		Sheet 30 of 52



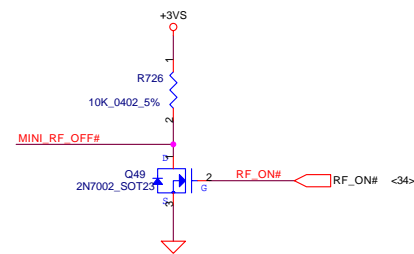
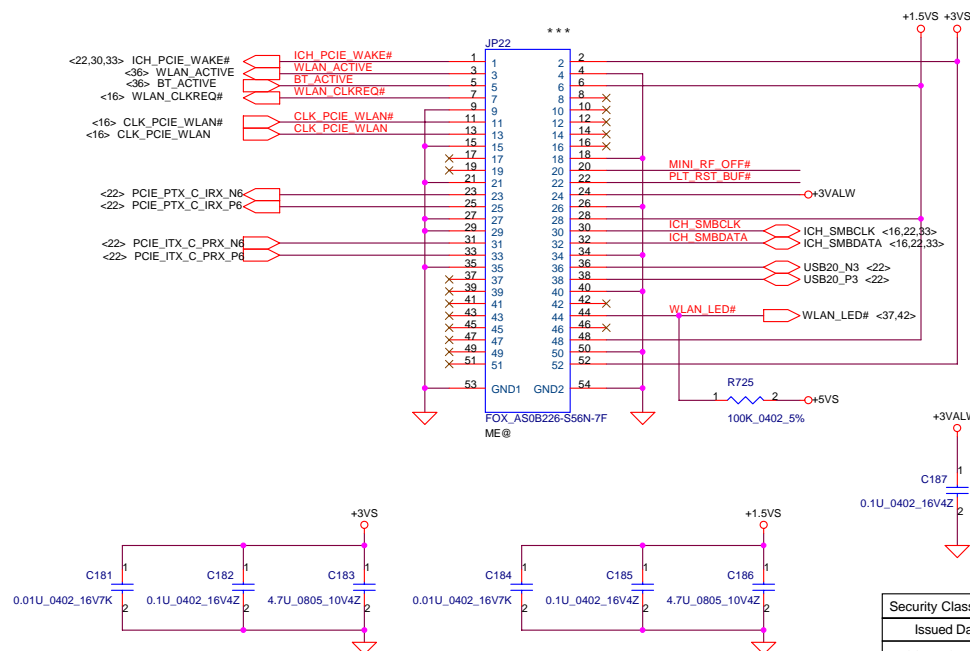
## NAND mini Card(Robson support)



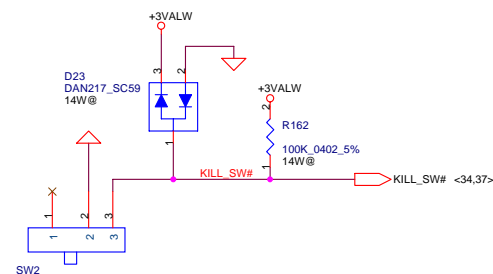
### Mini-Express Card for 3G Or TV Tuner



## Mini-Express Card for WLAN

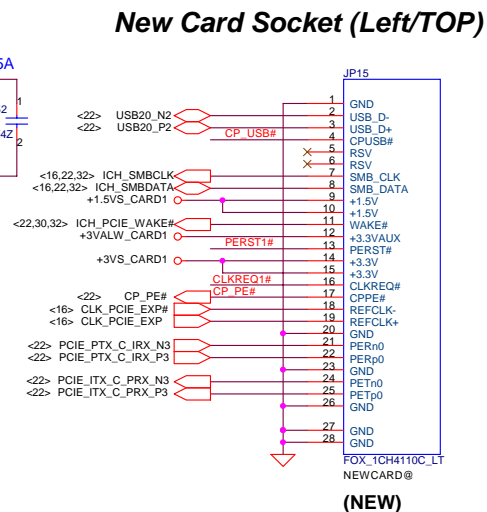
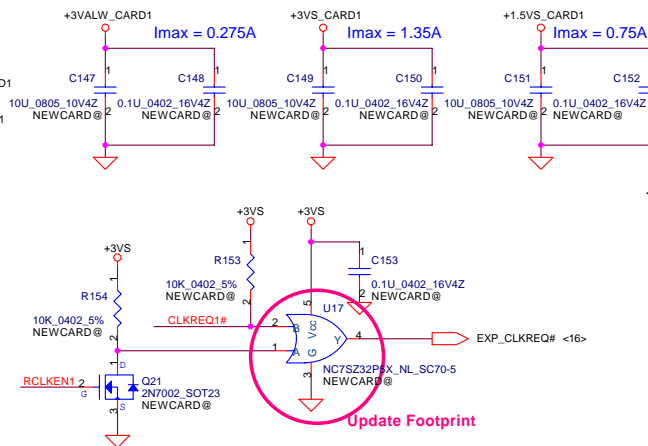
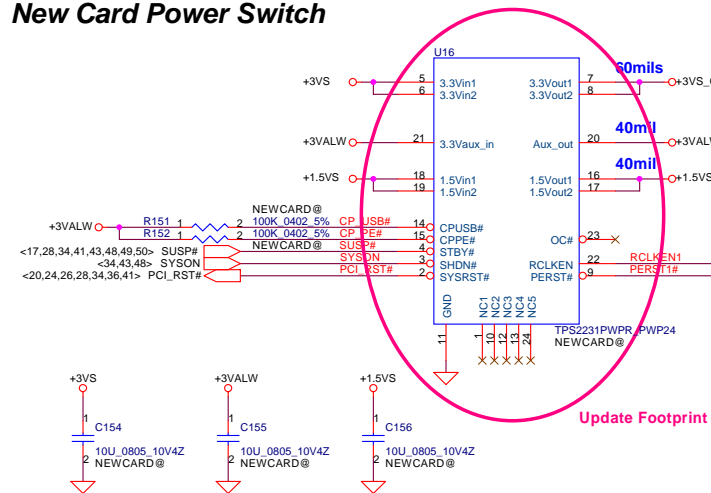


## Kill SWITCH

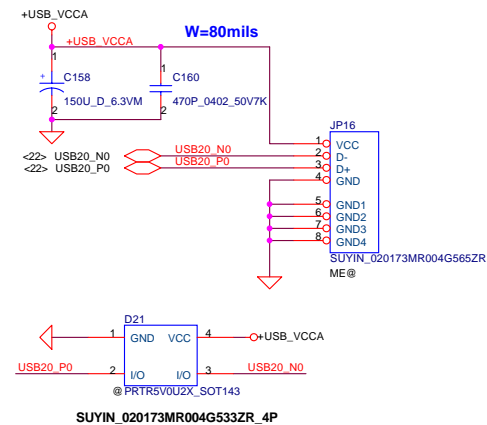


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>			
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title <b>Mini-Card/3G/FeliCa/FP</b>			
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					LA-3541P	0.1	
Date:				Wednesday, November 01, 2006	Sheet	32	of 52

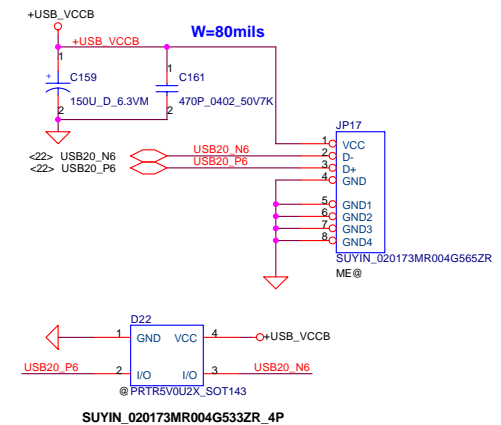
### ***New Card Power Switch***



**USB CONN. 1**



## USB CONN. 2



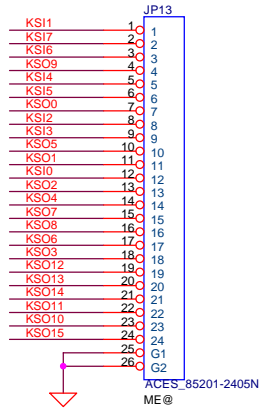
9/17 modified this block

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	NEW CARD & USB Connector		
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				B	IFTXX MB LA-3541P Schematic	0	
				Date:	Wednesday, November 01, 2006	Sheet	33 of 52

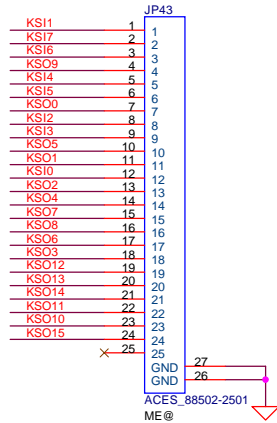


# INT\_KBD Conn.

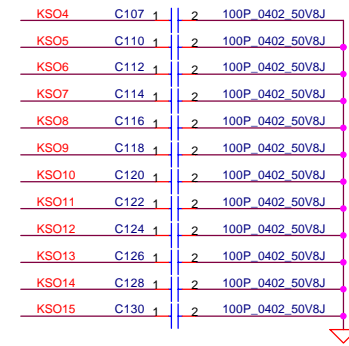
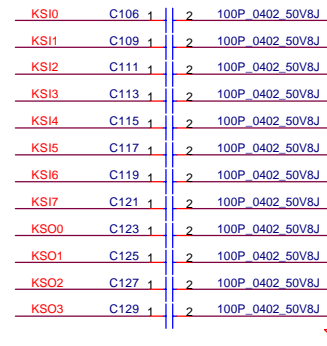
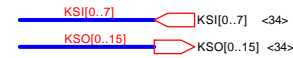
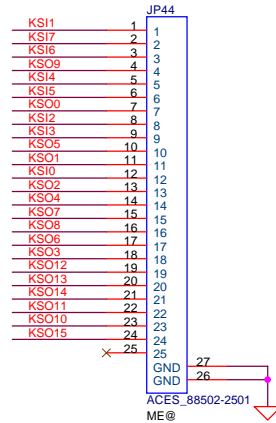
## For IFT10



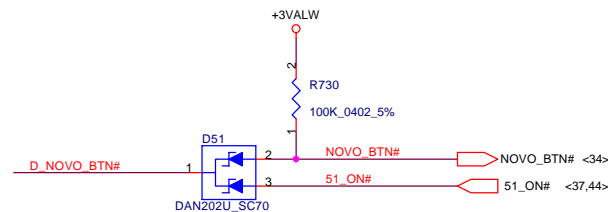
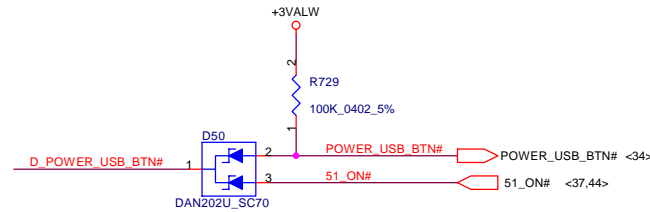
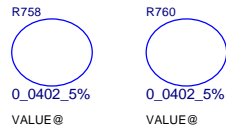
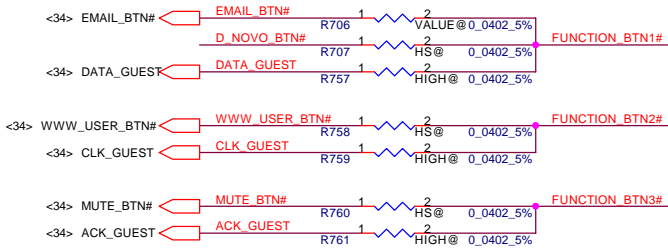
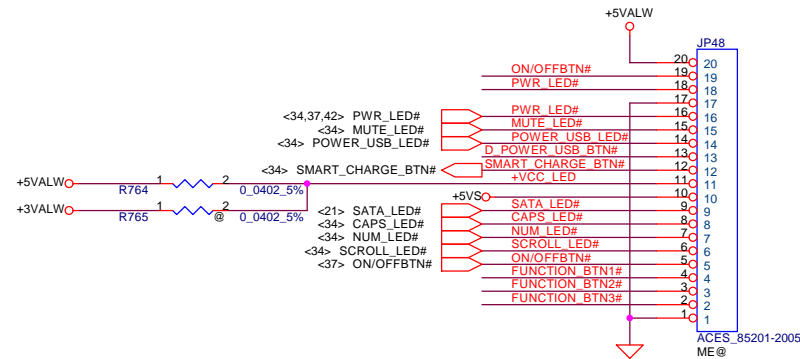
## For IFL90



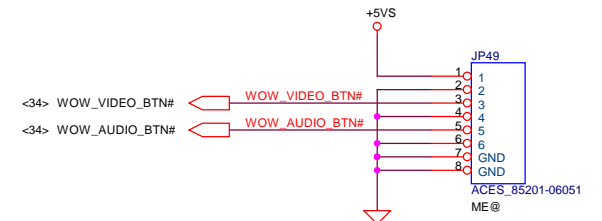
## For IFT00



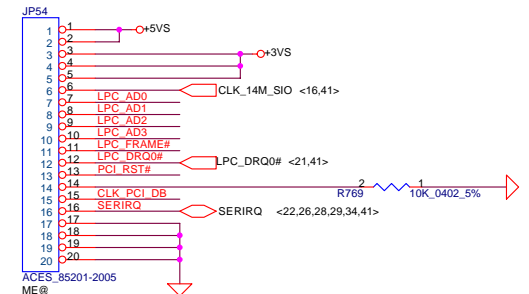
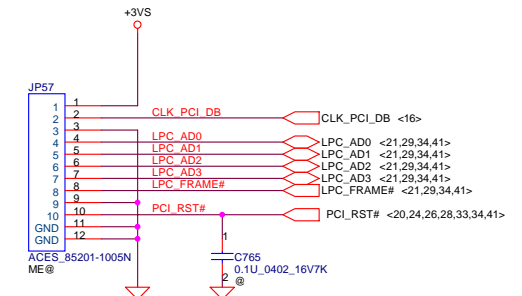
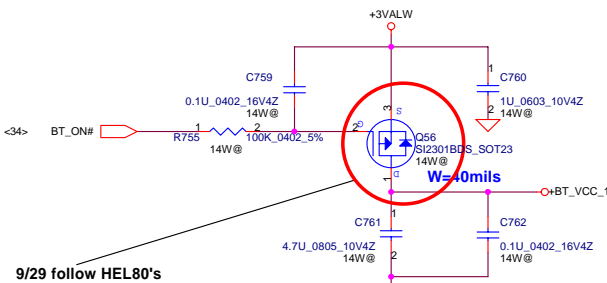
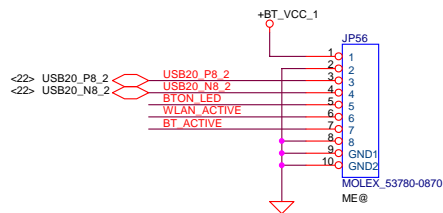
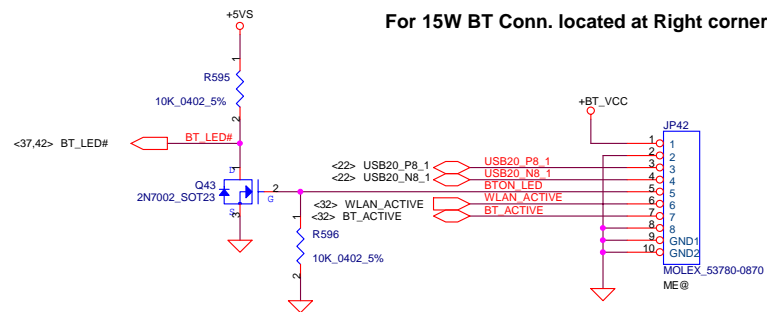
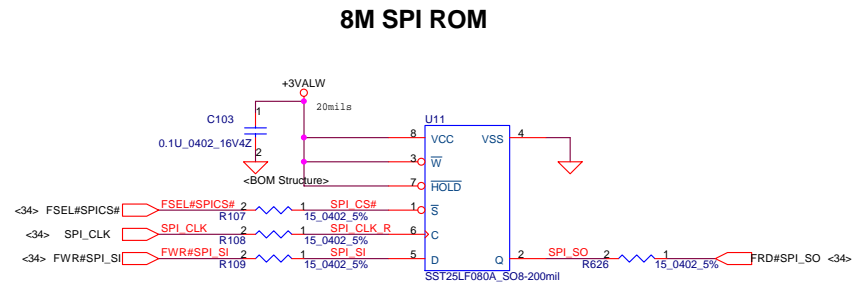
# Switch Board Conn.



# Video Switch Board Conn.



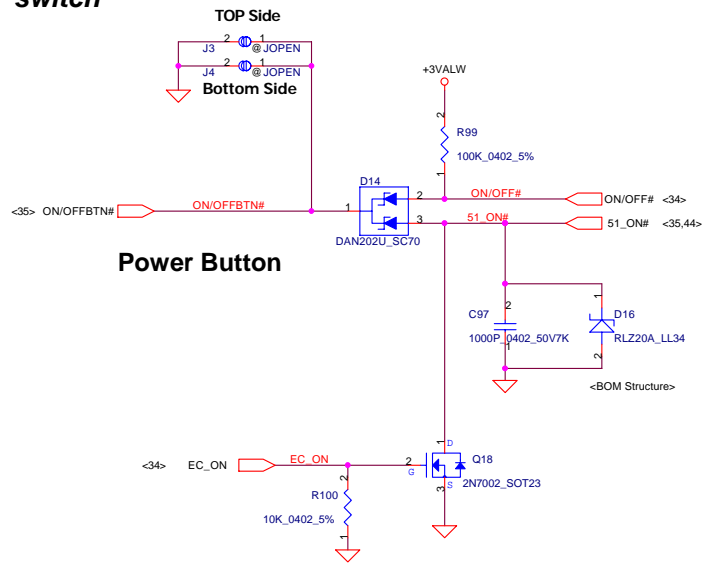
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Date:	Wednesday, November 01, 2006	Sheet	35	of	52



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				Size B	Document Number	Rev 0
				IFTXX M/B LA-3541P Schematic		
Date:				Wednesday, November 01, 2006	Sheet	36 of 52

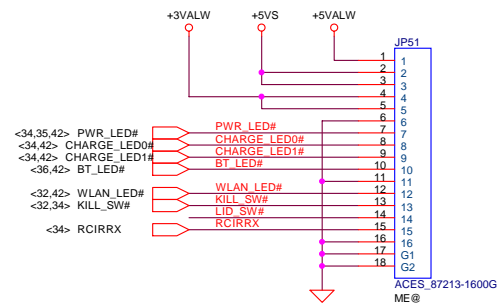


## ON/OFF switch

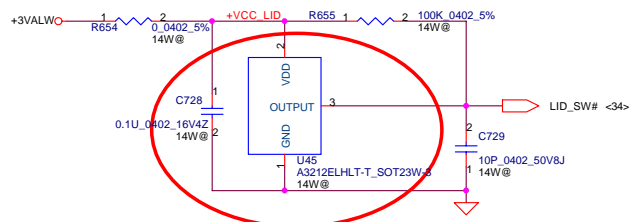


## Power Button

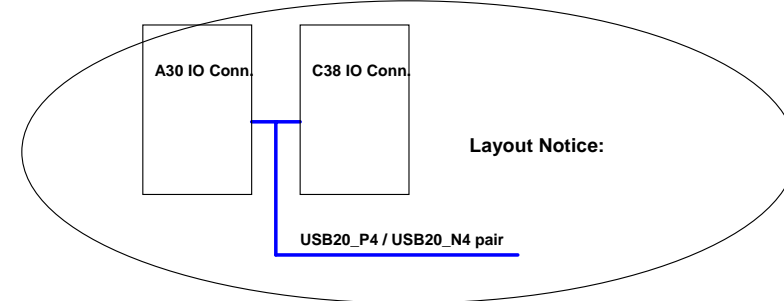
## Front LED Board



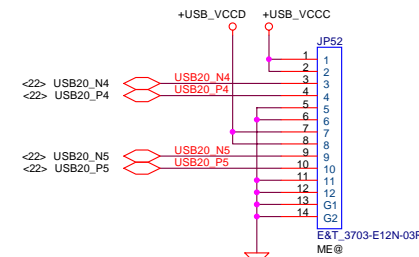
## Lid Switch



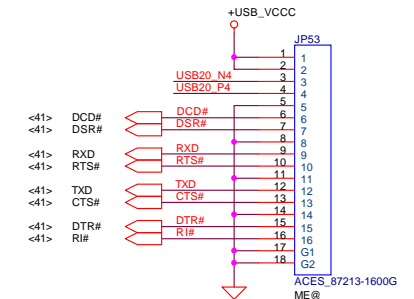
12/9 Change to SA032120010



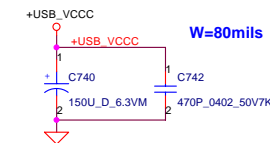
## For A30 IO Conn.



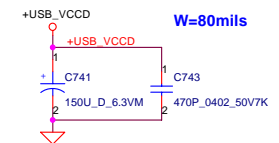
## For C38 IO Conn.



## To USB CONN. 3



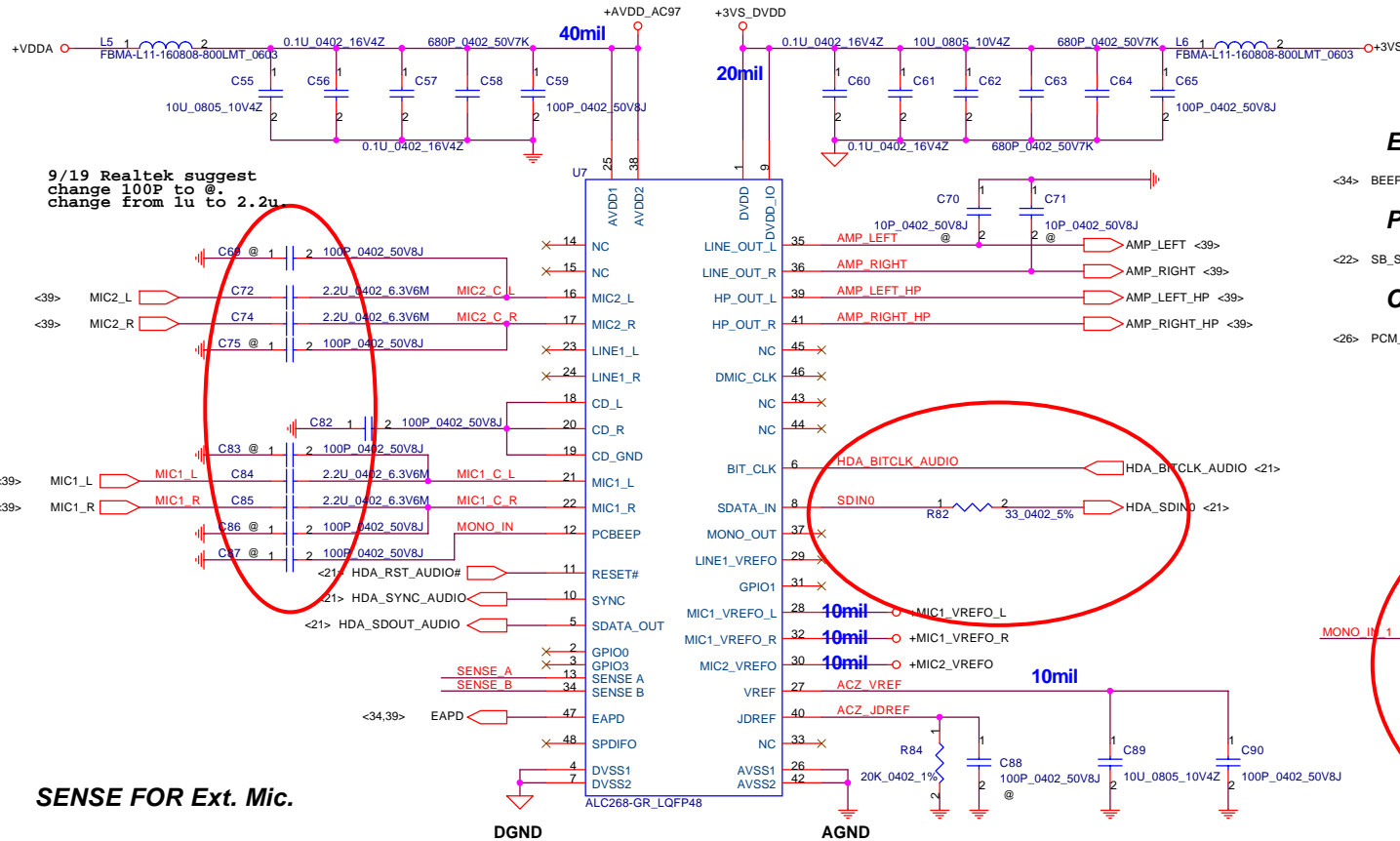
## To USB CONN. 4



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Power OK, Reset and RTC Circuit, TP			
Deciphered Date				2007/8/18				Size B			
Document Number				IFTXX MB LA-3541P Schematic				Date: Wednesday, November 01, 2006			
Sheet				37				Rev 0			

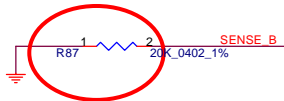
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## HD Audio Codec

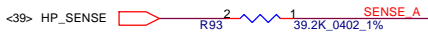


**SENSE FOR Ext. Mic.**

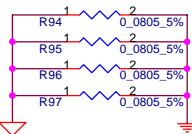
**SENSE FOR Solo Int. Mic.**



## SENSE FOR HP

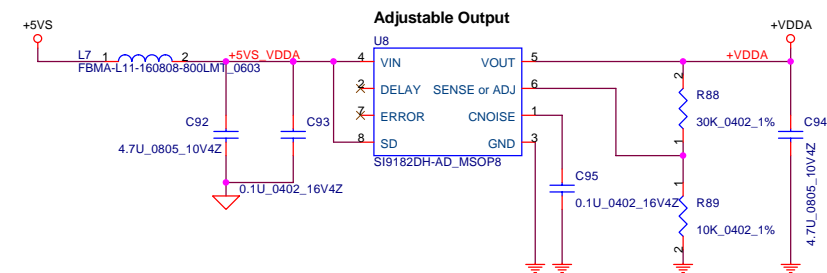


## Moat Bridge



Sense Pin	Impedance	Codec Signals	Funnnction
SENSE A / B	39.2K	PORT-A (PIN 39, 41)	HP
	20K	PORT-B (PIN 21, 22)	MIC
	10K	PORT-C (PIN 23, 24)	LINE IN
	5.1K	PORT-D (PIN 35, 36)	LINE Out
SENSE B	39.2K	PORT-E (PIN 14, 15)	HP
	20K	PORT-F (PIN 16, 17)	MIC
	10K	PORT-G (PIN 43, 44)	LINE IN
	5.1K	PORT-H (PIN 45, 46)	LINE Out

### Regulator for CODEC



9/22 Update footprint, Need to check

**EC Beep**

### PCI Beep

### ***CardBus Beep***

**Need Update Footprint**

9/19 Realtek suggest  
Add bypass schematic.

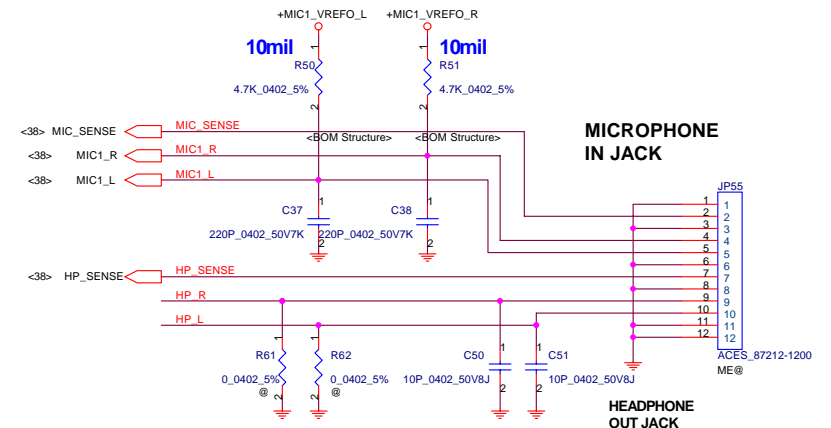
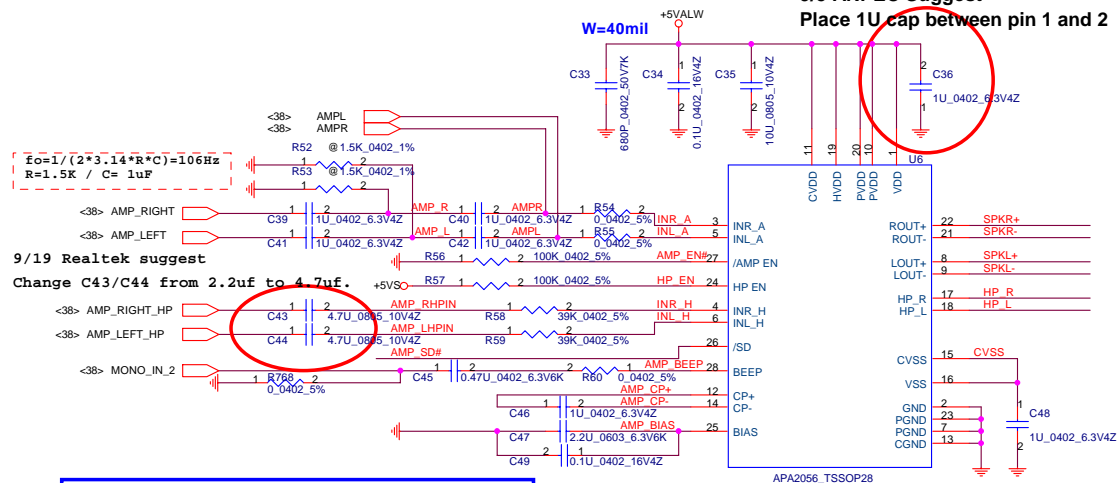
9/26 modified

### Adjustable Output

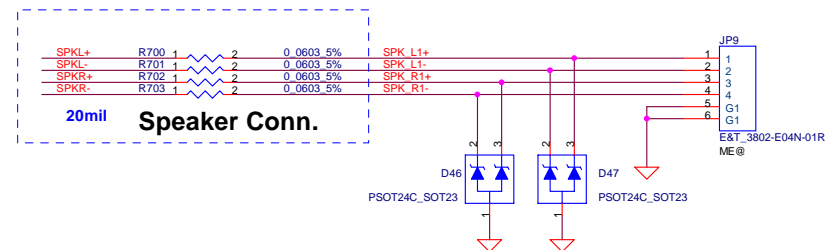
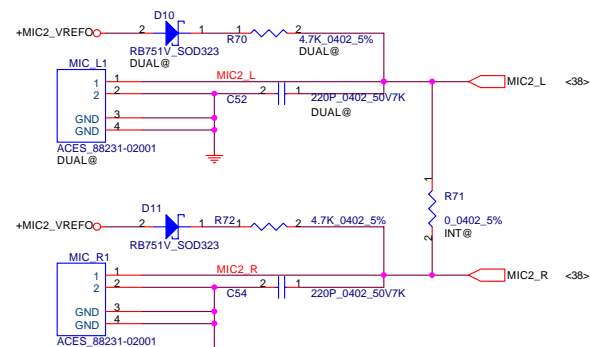
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2006/08/05	Deciphered Date	2007/08/05	Title	<Title> HD Audio Codec ALC268	
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				Cusom	LA-3541P	
				Date:		

# APA2056 SPK/HP Amplifier

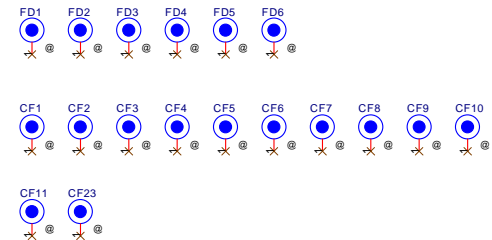
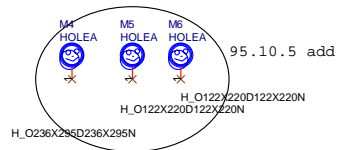
9/5 ANPEC Suggest  
Place 1U cap between pin 1 and 2



## SINGLE INT MIC/DUAL INT MIC

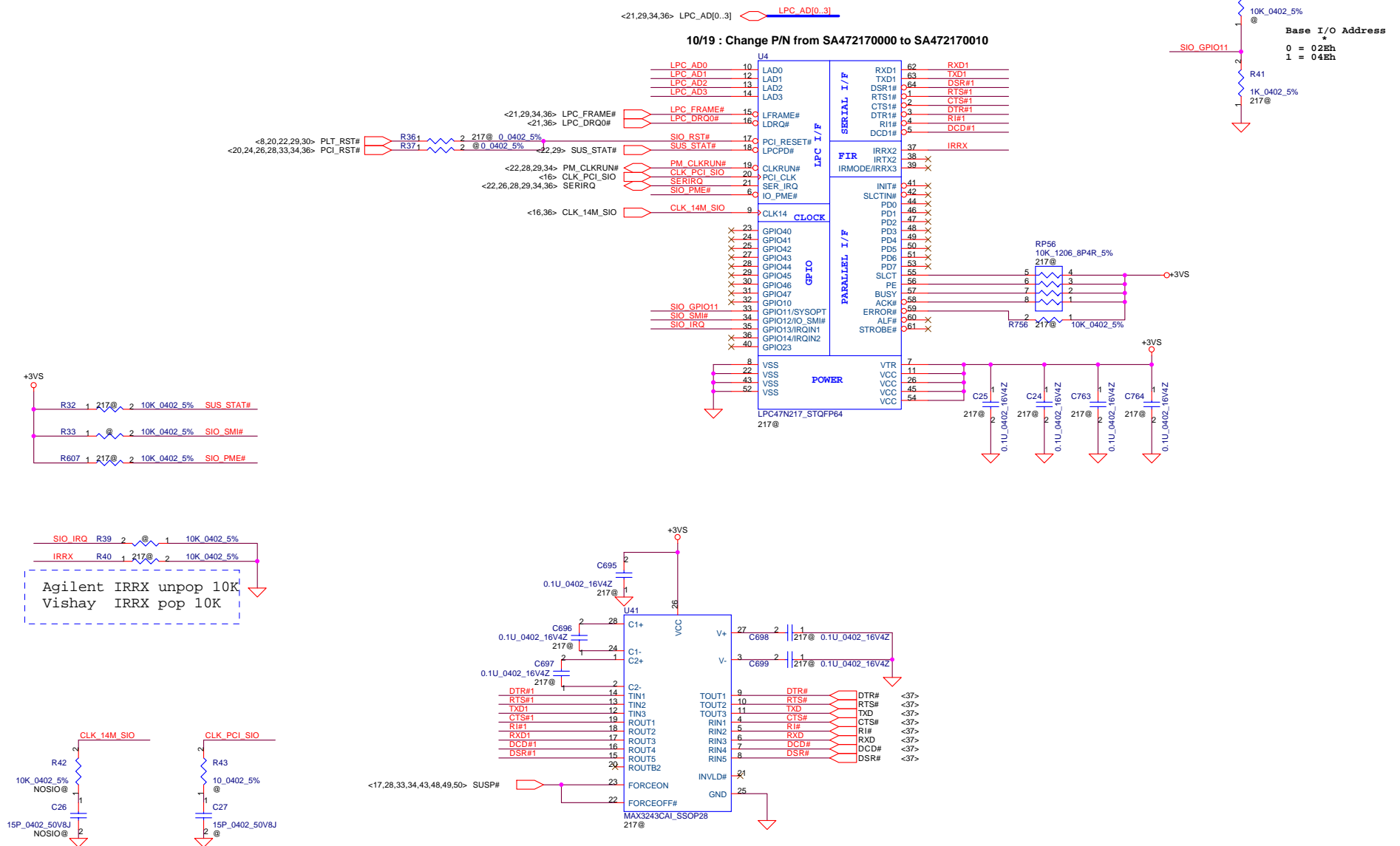


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Size	Document Number	Custpm		Rev	
	LA-3541P			0.1	
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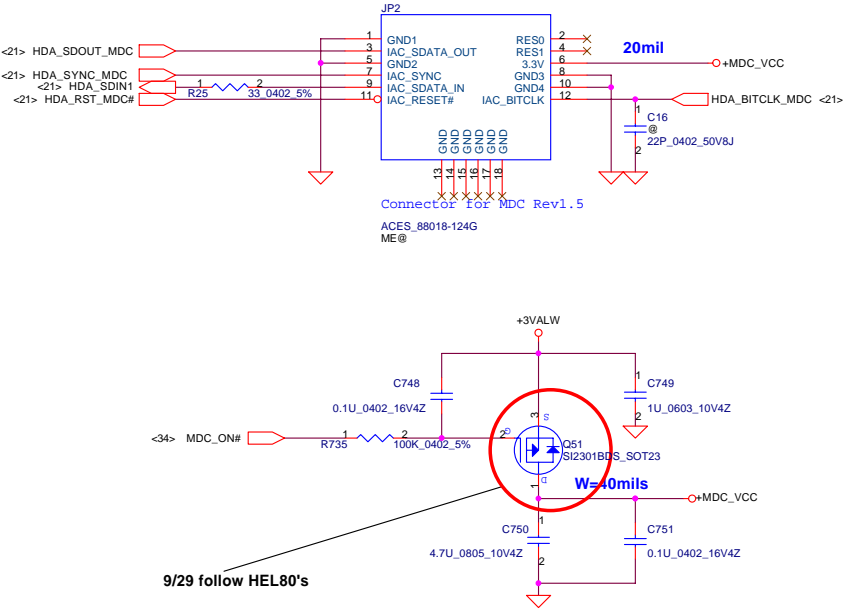
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	B	Document Number	IFTXX MB LA-3541P Schematic		Rev
Date:	Wednesday, November 01, 2006	Sheet	40	of	52

# SUPER I/O SMsC LPC47N217

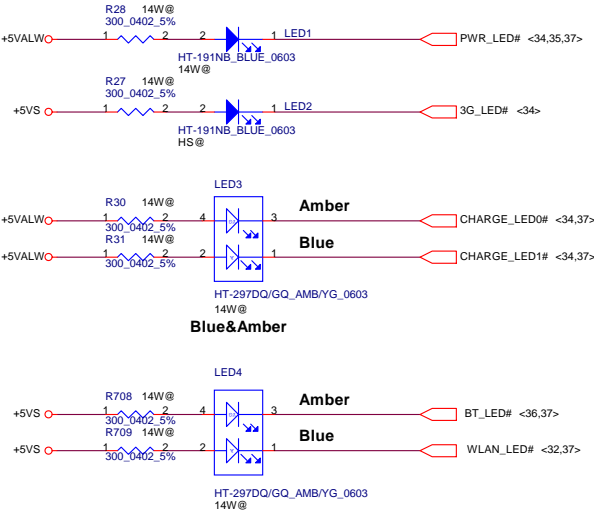


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/05/26	Deciphered Date	2006/07/26	Title	
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Size	Document Number	LA-3541P UMA		Rev	0.2
Date:	Wednesday, November 01, 2006	Sheet	41 of 52	Rev	

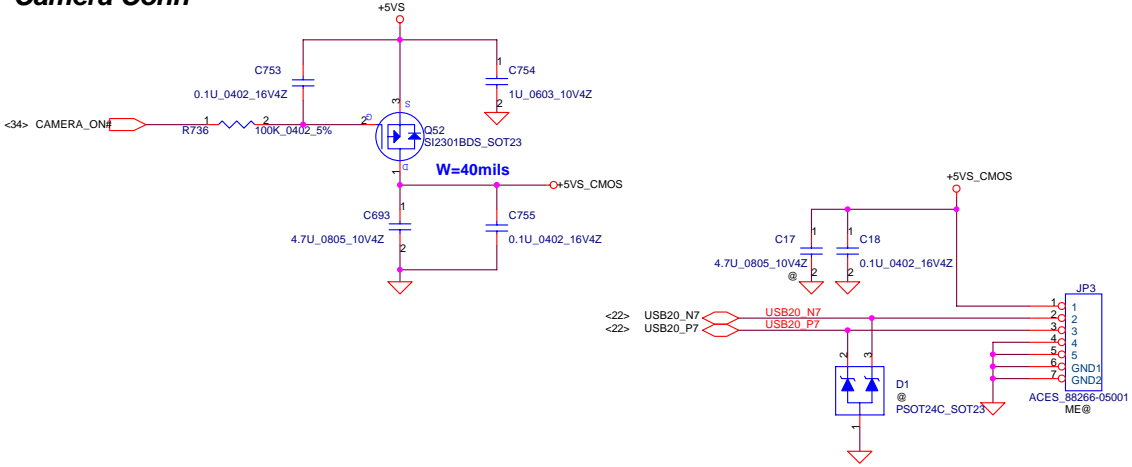
MDC Conn.



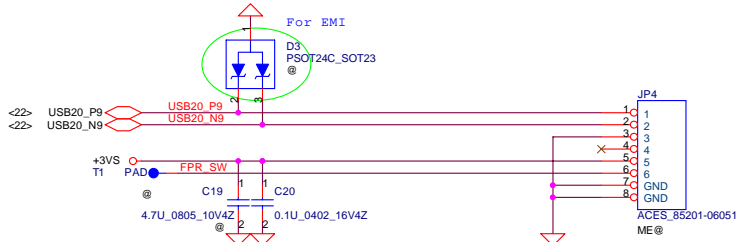
LED



Camera Conn

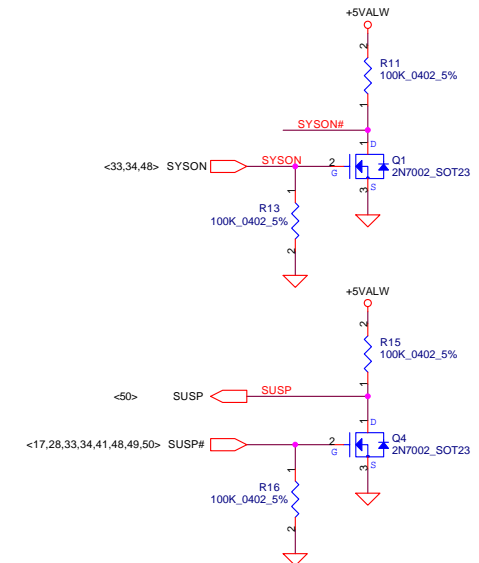
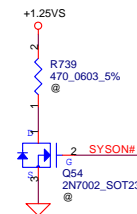
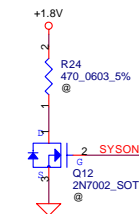
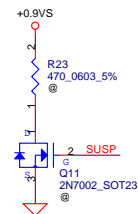
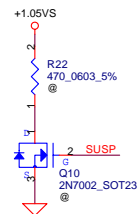
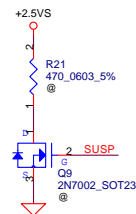
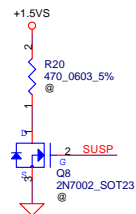
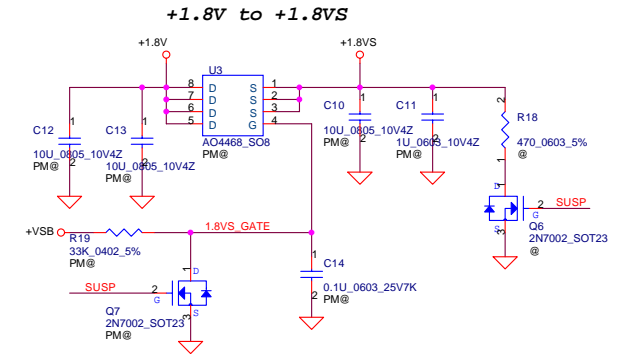
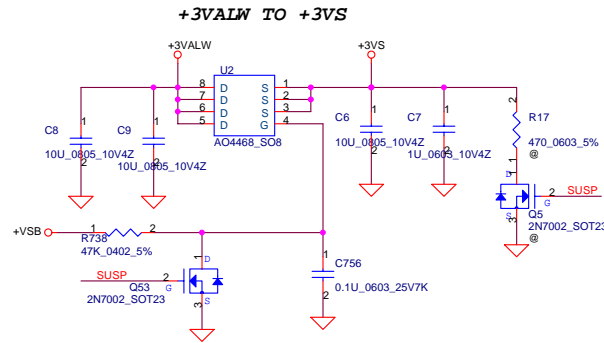
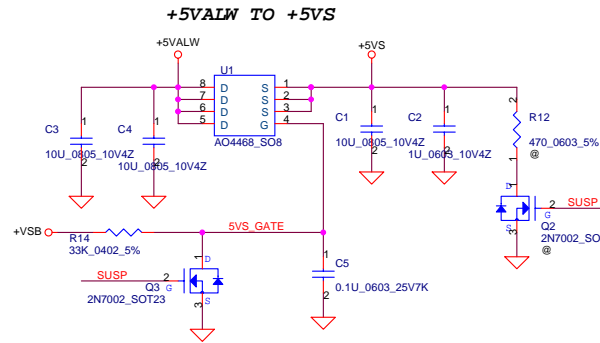


Finger Print board



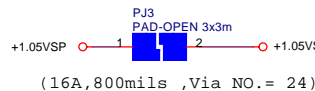
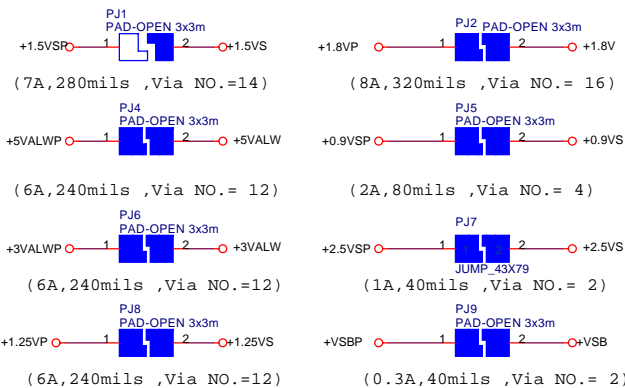
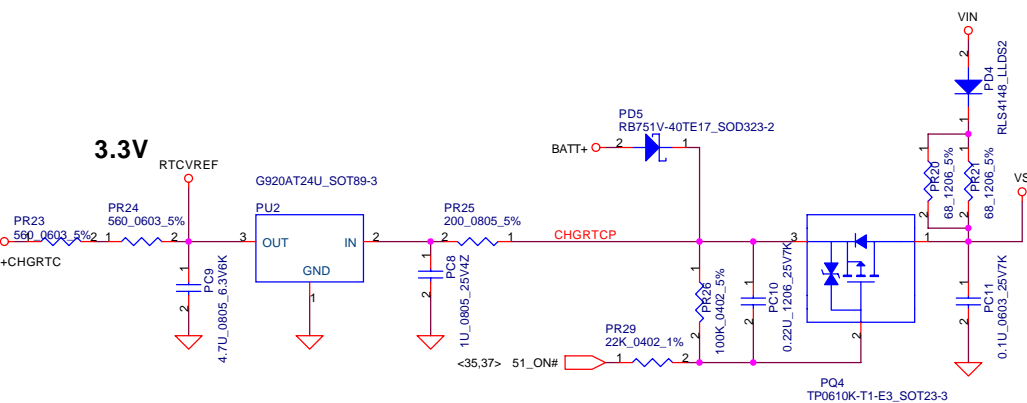
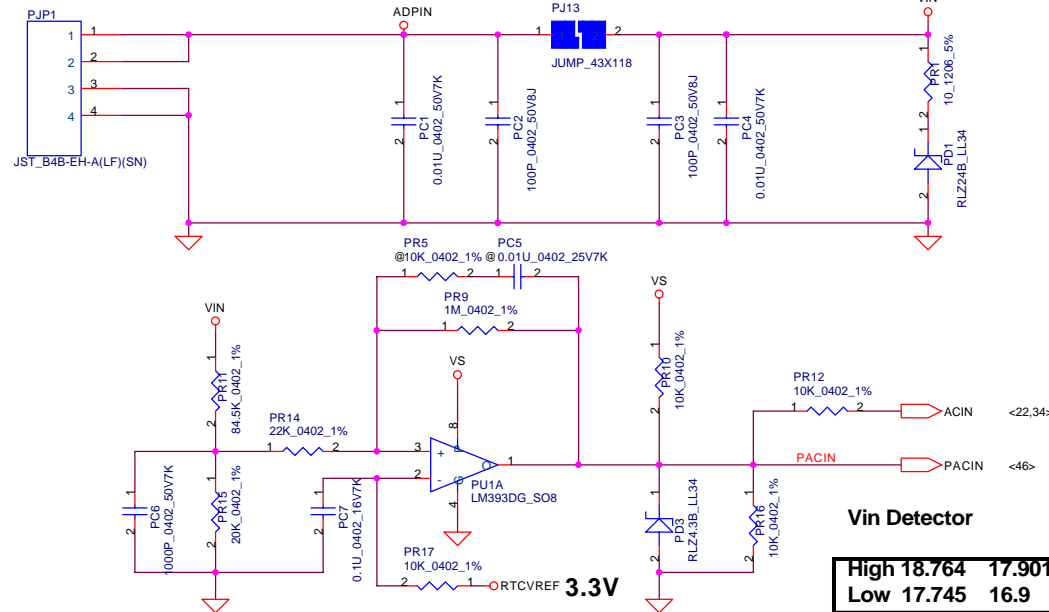
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Issued Date		2006/08/18		Deciphered Date		2007/8/18		Title					
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								Size	Document Number				Rev
								B	IFTXX M/B LA-3541P Schematic				0
								Date:	Wednesday, November 01, 2006		Sheet	42	of





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Size B	Document Number	IFTXX/MB LA-3541P Schematic			Rev 0
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DC030005Q00

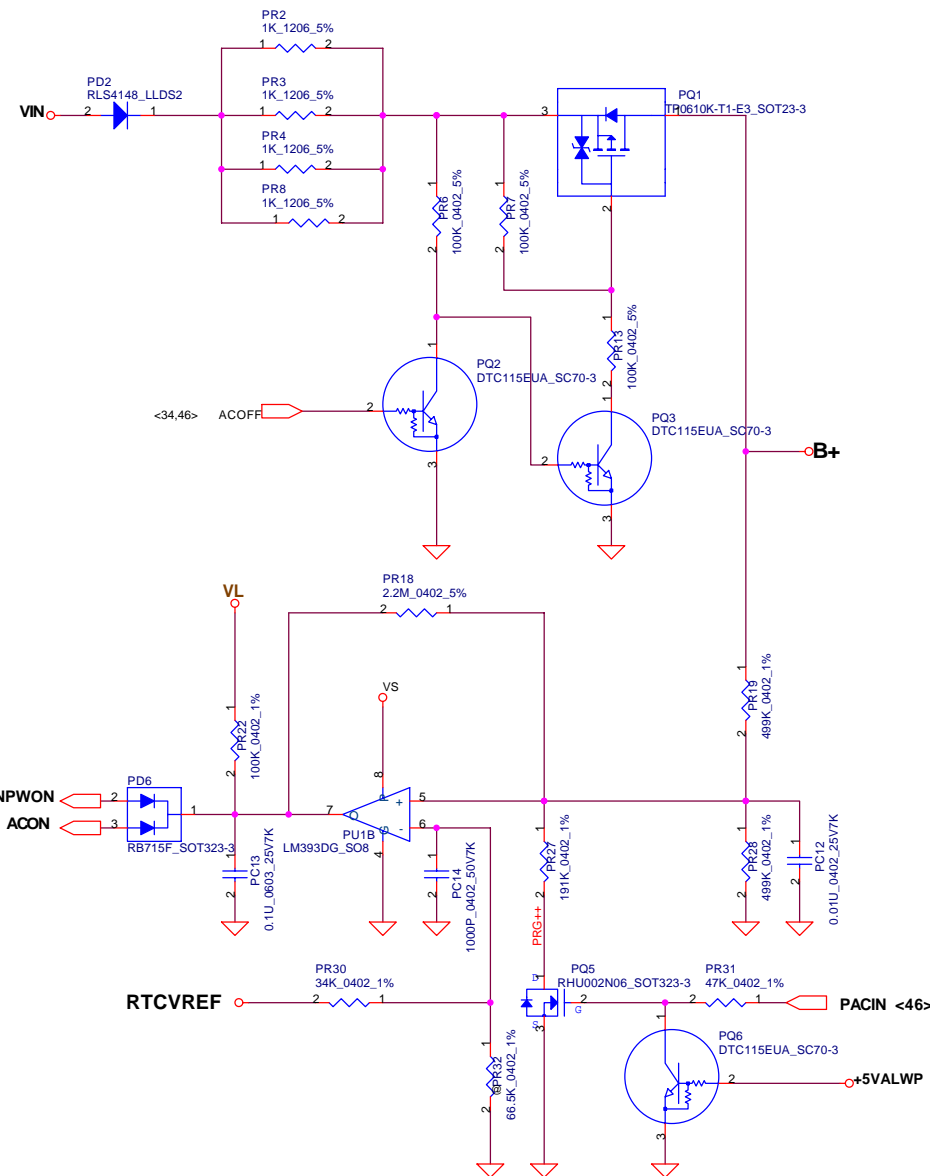


ACIN

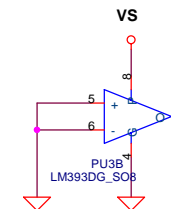
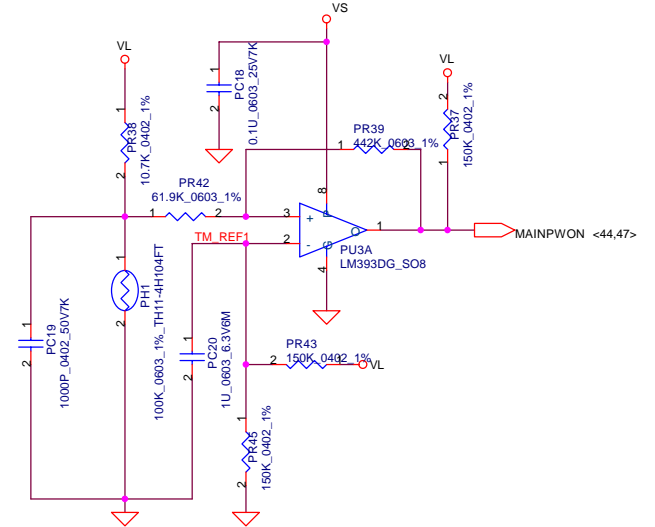
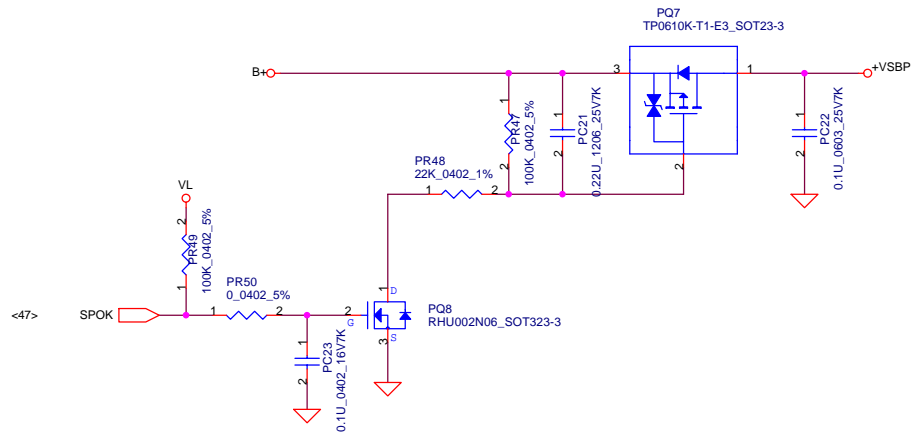
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

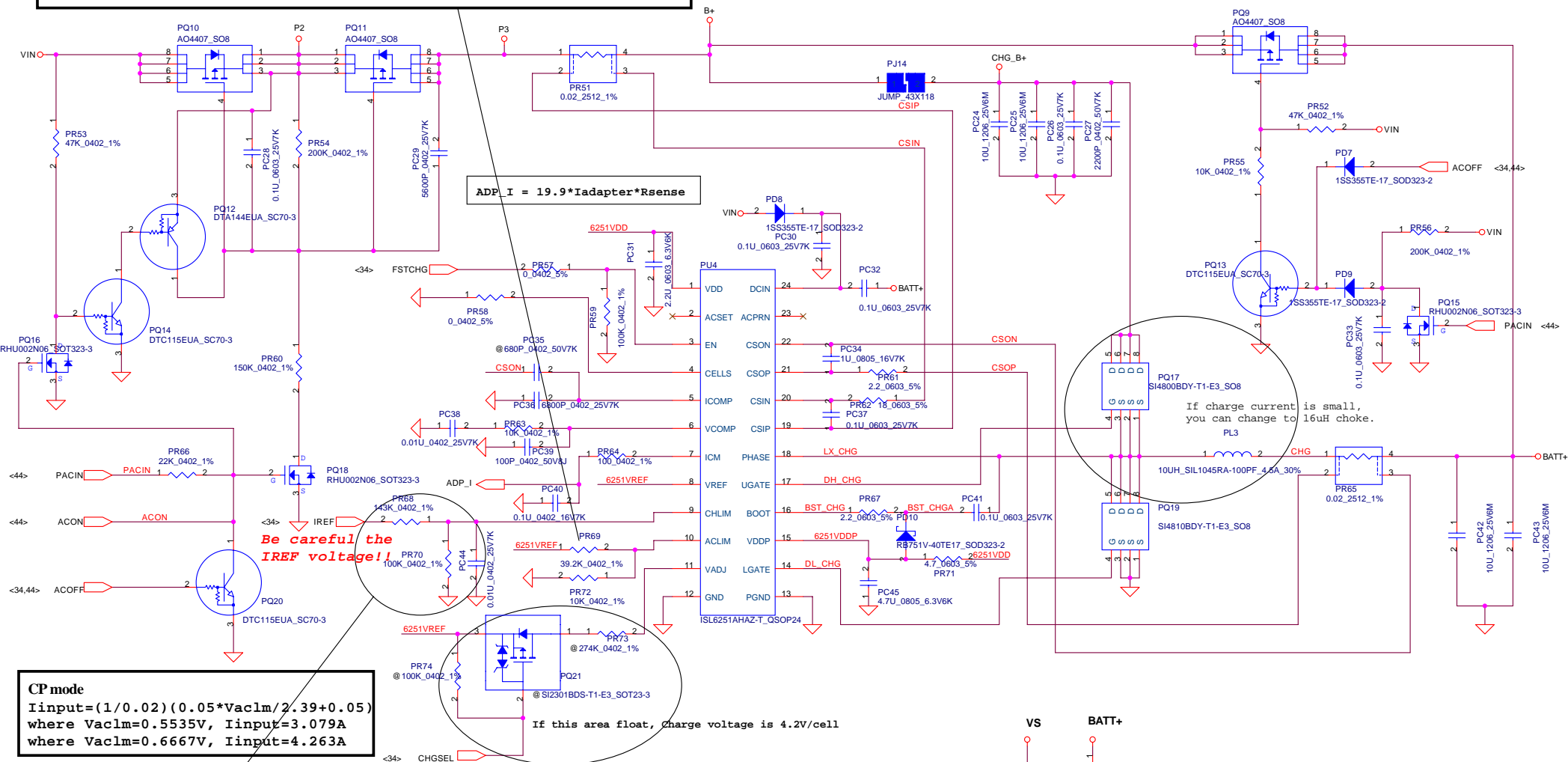


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Size				B				Rev			
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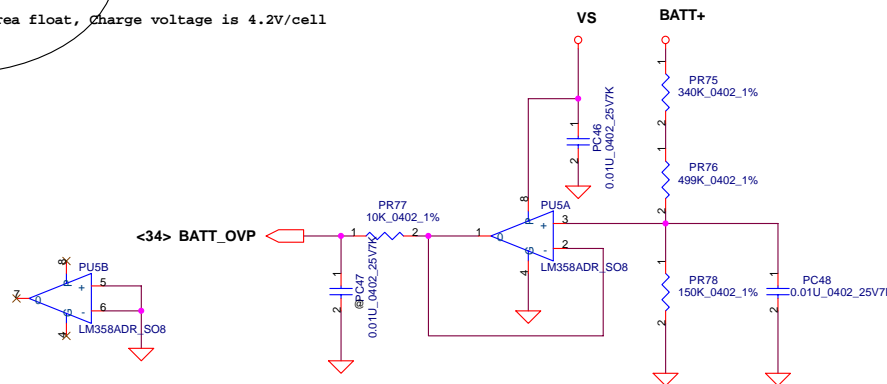
65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR69=39.2K, CP=3.079A  
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR69=28.7K, CP=4.263A

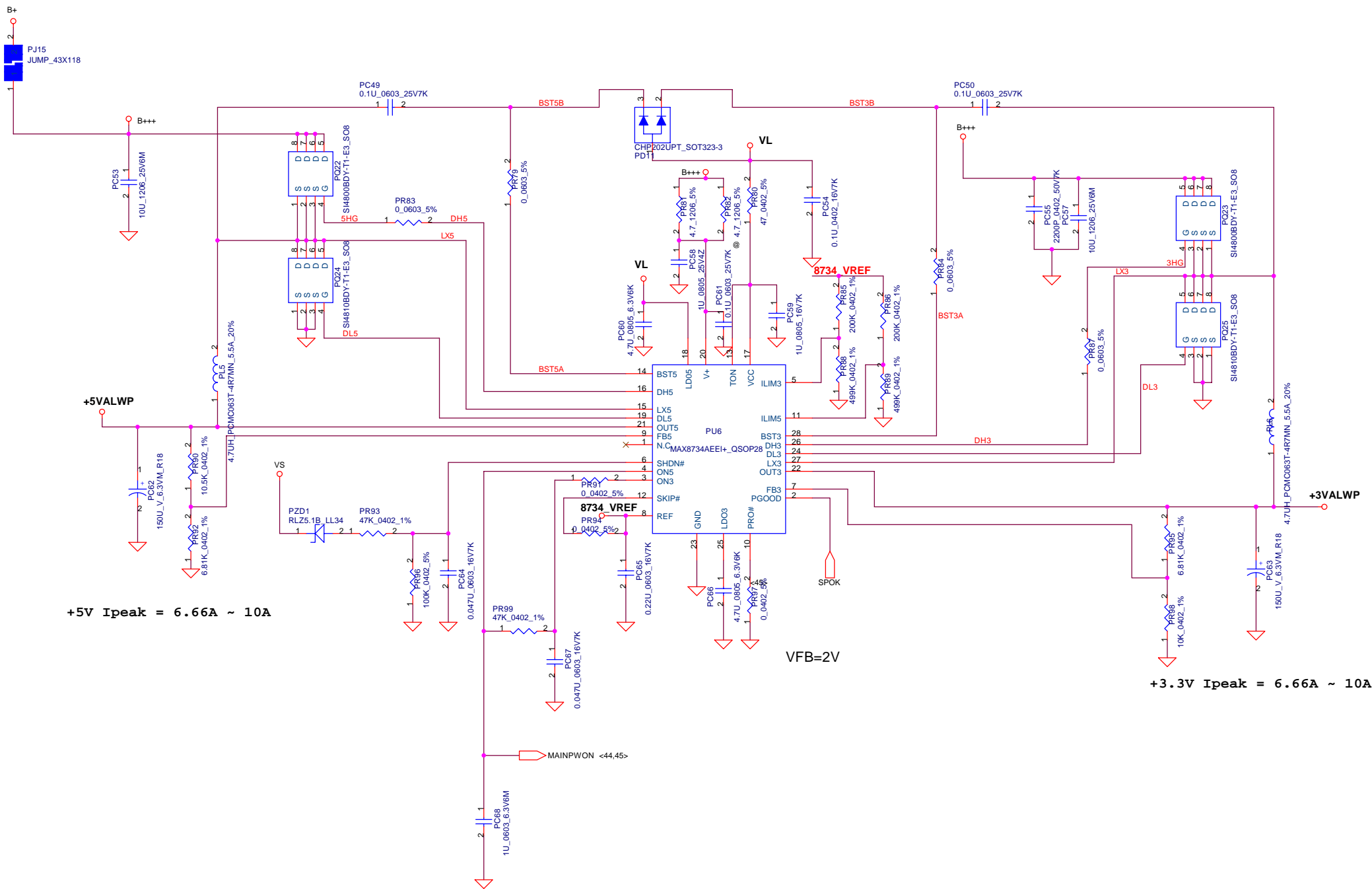


**CP mode**  
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$   
 where  $V_{ac1m} = 0.5535V$ ,  $I_{input} = 3.079A$   
 where  $V_{ac1m} = 0.6667V$ ,  $I_{input} = 4.263A$

**CC=0.6~3.4A**  
 $V_{CHLM} = 0.24V \sim 1.36V$   
 $I_{REF} = 0.972 * I_{charge}$   
 $I_{REF} = 0.5832V \sim 3.3V$

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V



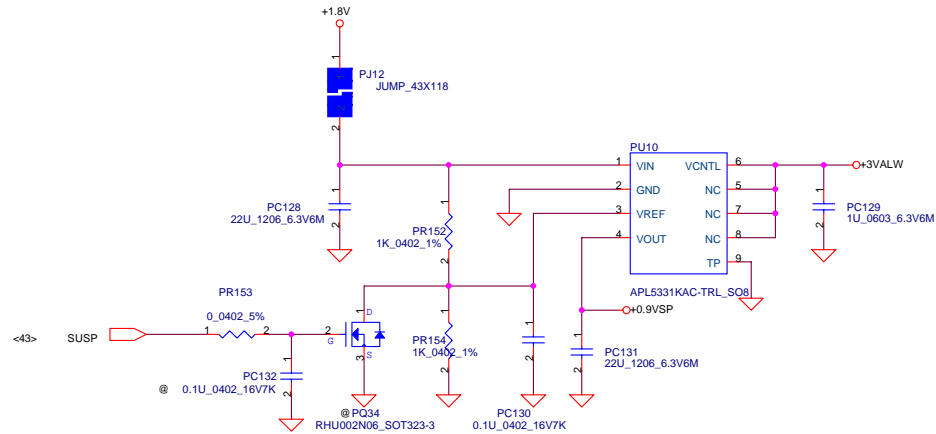
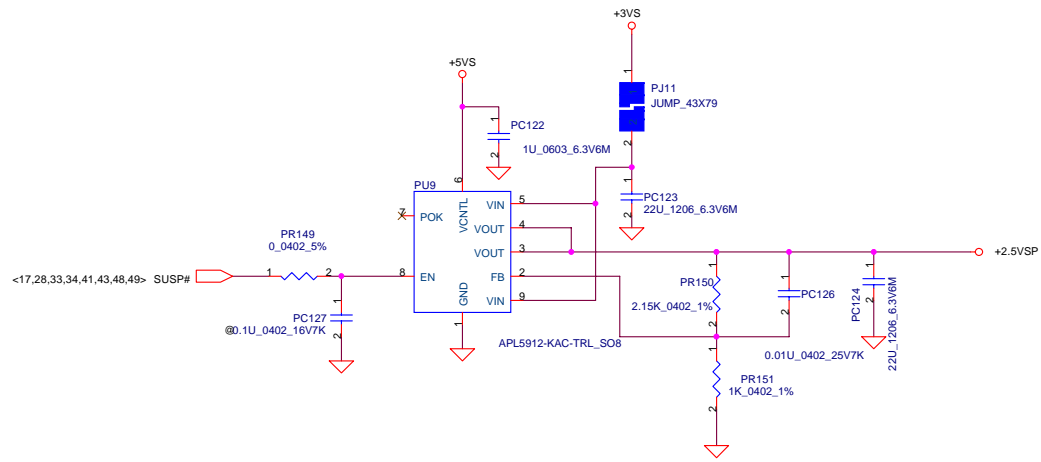


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page

Reason for change

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